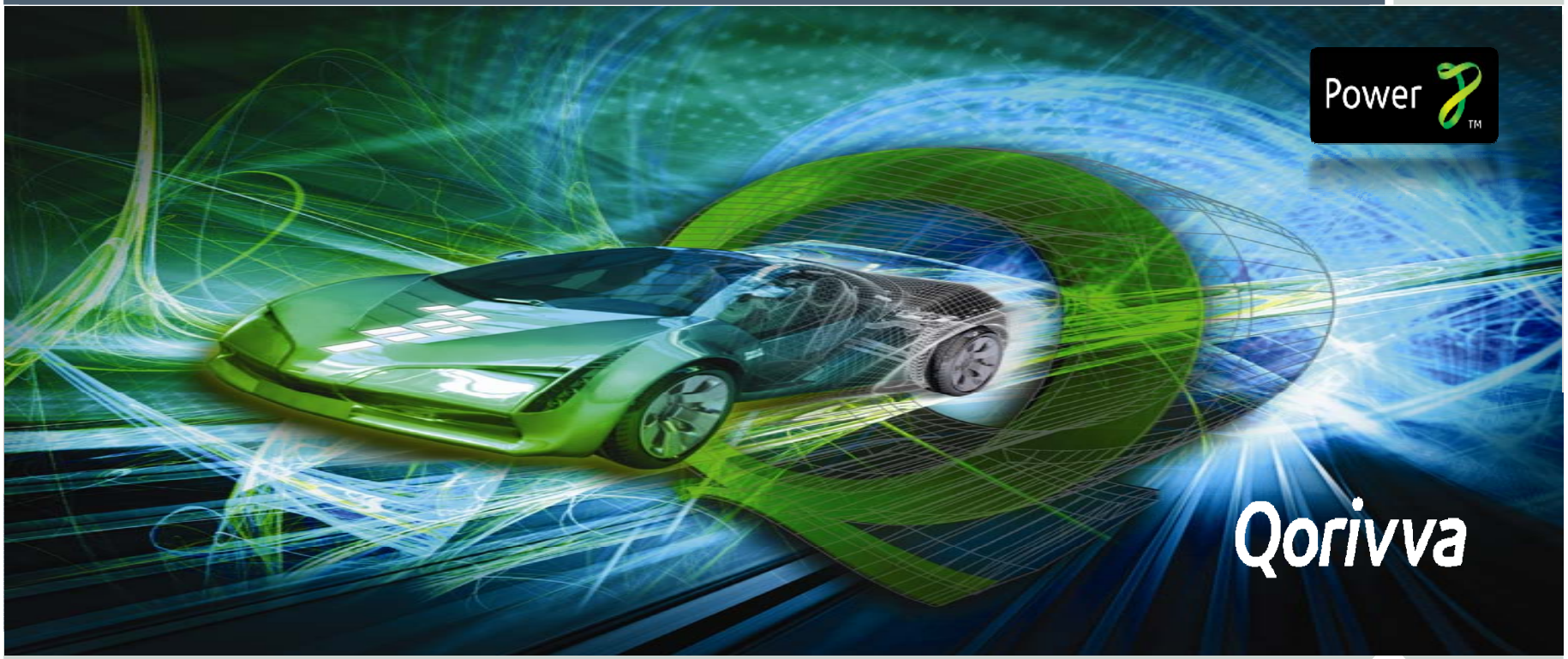

June.8th.2011

Qorivva: 32-bit Power Architecture™ MCU

DwF(Hangzhou) Hands-on Training

Johnny Chen 陈东华

Automotive Field Application Engineer

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Agenda

1. Qorivva Device Overview -Bolero/Pictus/Spectrum/Monaco -Development Tools and Support	***6. Interrupt Control*** - Hardware vector mode - Software vector mode - Hands-on: SW-Interrupt
2. I/O Modules – SIUL - Hands-On: EVB intro; GPIO;	***7. Communication Modules*** - DSPI - LINFlex - FlexCAN/CAN Sampler -Hands-On: RappID&FlexCAN
3. System Clock Module/Timer - FIRC/FXOSC/SIRC/SXOSC/PLL - STM/RTC/SWT/PIT - Hands-On: System_Clk	***8. System Related*** - Peripheral Bridge - Crossbar Switch - BAM
4. Power Mode Control - Mode Entry Module - Power Control Unit - Voltage Regulator - Wakeup Unit - Hands-on: Mode-Transition, Standby	***9.*** ADC/CTU/EMIOS - ADC - CTU - EMIOS - Hands-on: ADC-EMIOS
5. Memory - Memory Map - Flash/SRAM - MPU	***10.*** Hands-on Workshop - Starter TRAK - Lab Demo 1,2,3,4,5,6,7

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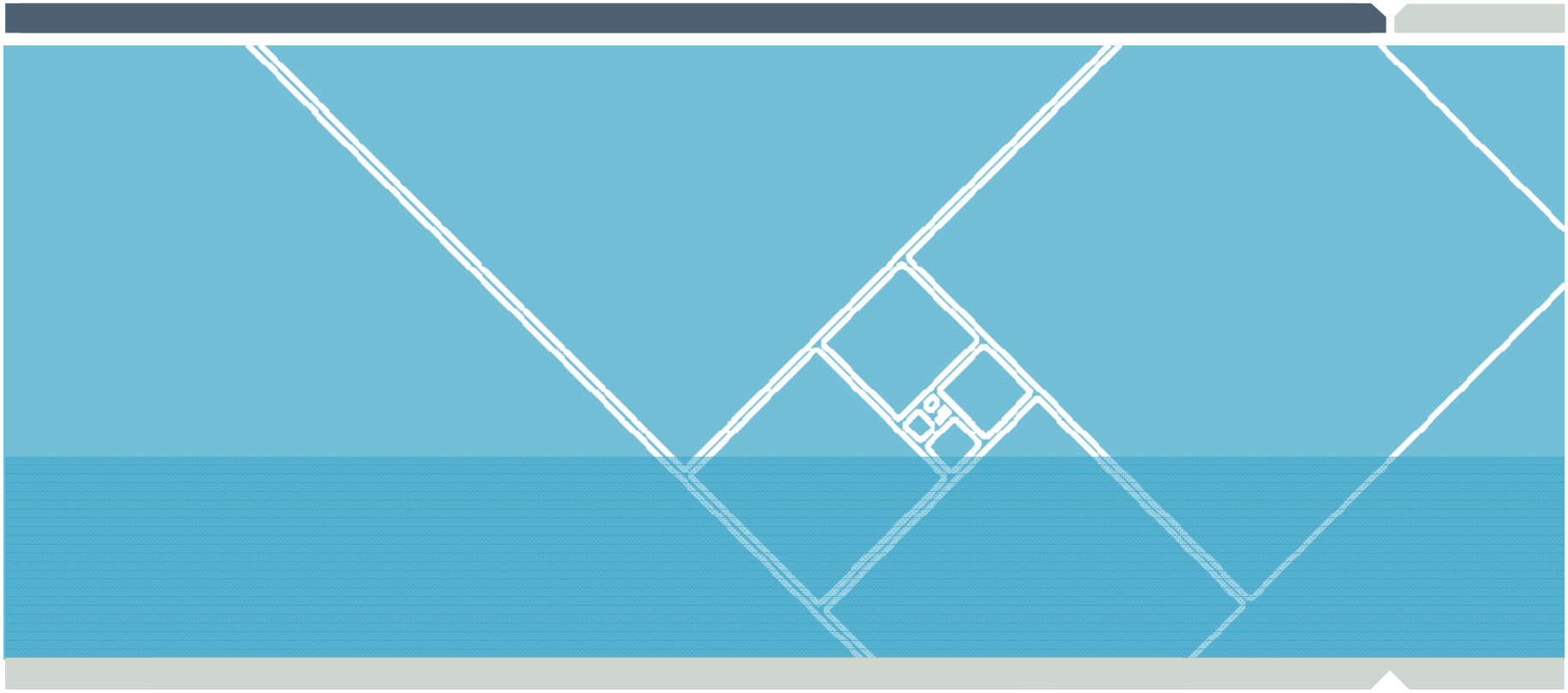

1. Qorivva(MPC56xx) Device Overview

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What's a Power Architecture™ MCU?

An industry benchmark architecture, very successful in embedded systems from automotive powertrain, navigation systems to netcom applications

A long term partnership between FSL and IBM

The 32bit architecture of choice for FSL in automotive applications

Single issue, multiple execution unit, 32 bit RISC CPU

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Why 32bit?

- Evolving software development methodologies
  - More structured software architectures engineered for reuse creating overhead
    Example: AUTOSAR standardization adding about 10-15% performance overhead.
  - Linear paged architecture and 32bit data handling allows for easier implementation of model-based designs and autocoding.

- Scalability upwards allowing platform designs from low- to high-end systems.

- More affordable as technology shrinks the cost delta between 32bit and 16bit architectures reduces.

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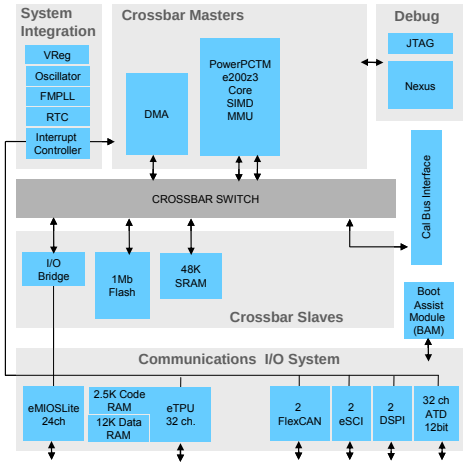
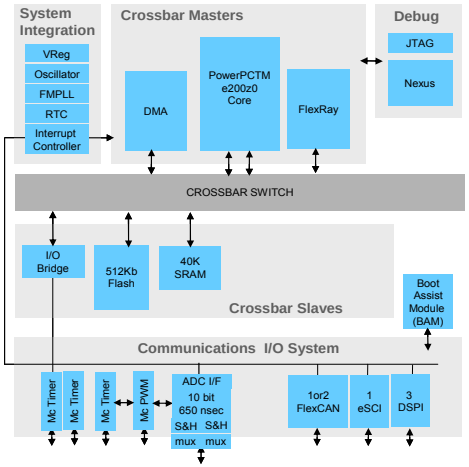
Cross-Family Compatibility

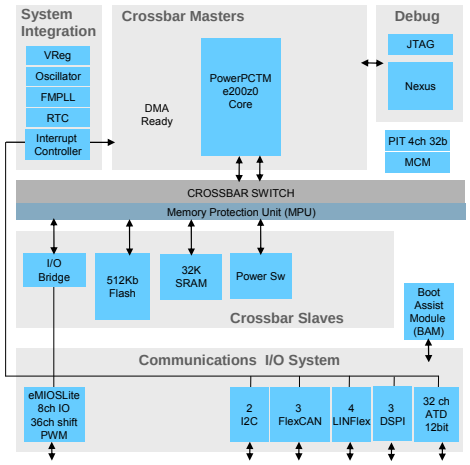
MPC563xM
(Powertrain)



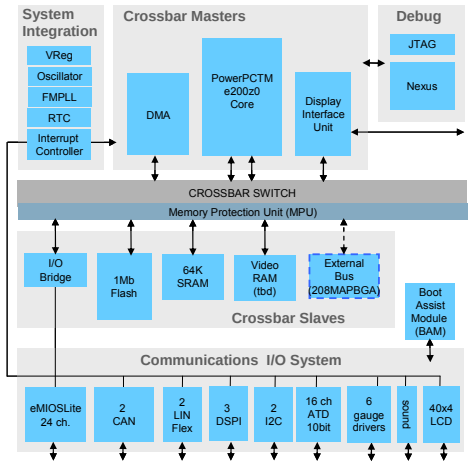
MPC560xP
(Airbag/Steering)



MPC560xB/C
(Body)



MPC560xS
(Instrument Cluster)



32-bit standard architecture adopted across all product families

- **Maximum IP reuse**
- **Faster time-to-market**
- **Reduced risk**
- **Leverage software and tools investments**

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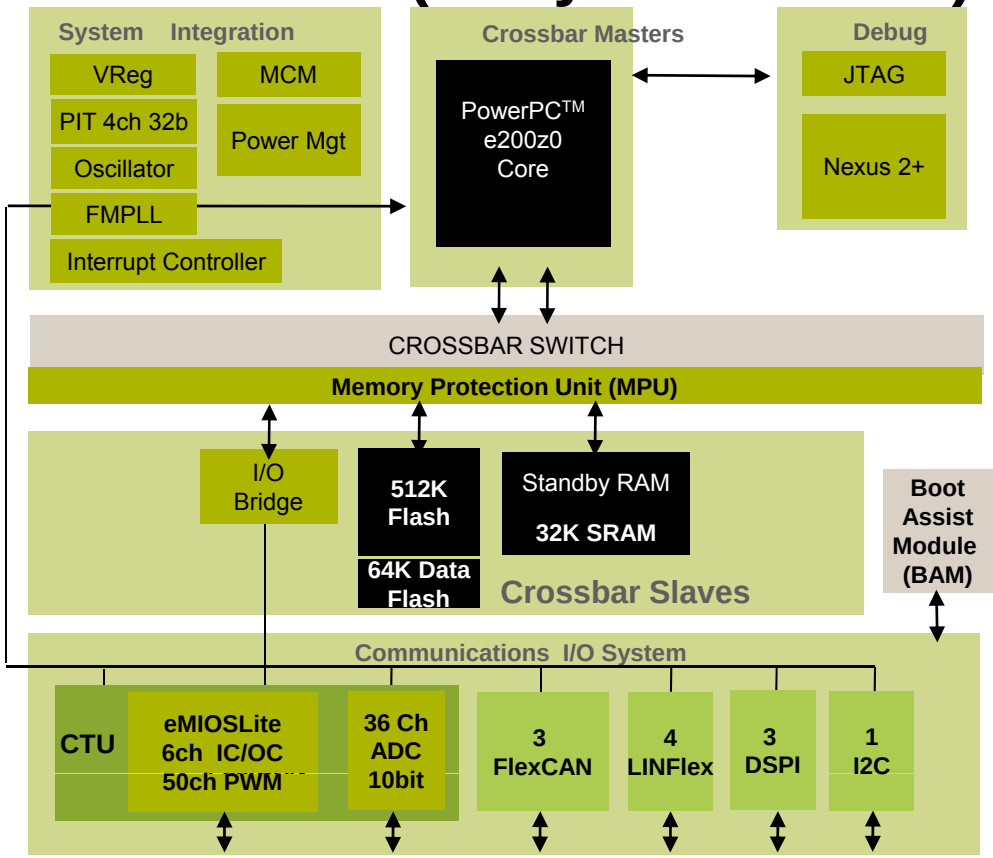
MPC560xB/C (Body Electronics)

Family Overview

- Targeted at mid-range complex control and diagnostic applications, such as central body, gateway, and comfort
- FlexCAN module supporting both FIFO and mailbox data storage, ideal for Controller Area Network (CAN) gateways to manage event driven vs. periodic bus traffic
- LINFlex module provides a fully automated Local Interconnect Network (LIN) message management, reducing CPU load intervention and message latencies
- eMIOS timer combines multiple counter sources to input capture, output compare and PWM capabilities in one very flexible module; PWM function supports shifted signal output to improve EMC
- Cross Triggering Unit (CTU) synchronizes PWM output signals with analog-to-digital conversions
- Enables very accurate diagnostic and control capabilities



Note: block diagram represents the MPC5606B

Family Differences

Device	Flash	SRAM	SCI (LINFlex)	CAN (FlexCAN)	Pins
MPC5604B	512KB	32KB	4	3	64, 100, 144, 208 (Emul. Only)
MPC5603B	384KB	28KB	4	3	64, 100, 144
MPC5602B	256KB	24KB	3	2	64, 100, 144

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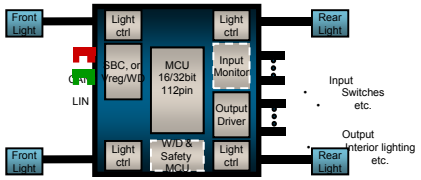
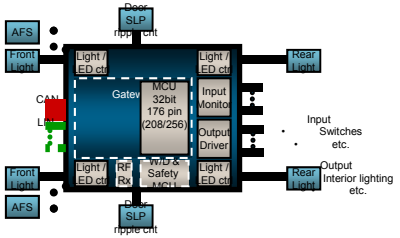
Bolero Family Product Offering

Entry Level BCM



Mid-Range BCM



Applications	Basic functions, e.g. lighting, immobilizer, power management	+ multiple CAN + other peripheral functions, e.g. doors, seats
Feature Needs	16/32bit MCU <512k Flash 1-2 CAN 1-2 LIN <112 LQFP	1 x 16/32bit MCU <1.5MB Flash 3-4 CAN 7 LIN 144/176 LQFP
Freescale Solution	**MPC5604/3/2B/C** z0 64MHz Up to 512KB Flash, 48KB RAM Up to 6 CAN, 4 LIN, 3 SPI 100-144 Pin	**MPC5607/6/5B** z0 64MHz Up to 1.5M Flash, 96KB RAM Up to 6 CAN, 10 LIN, 6 SPI 100-176 Pin

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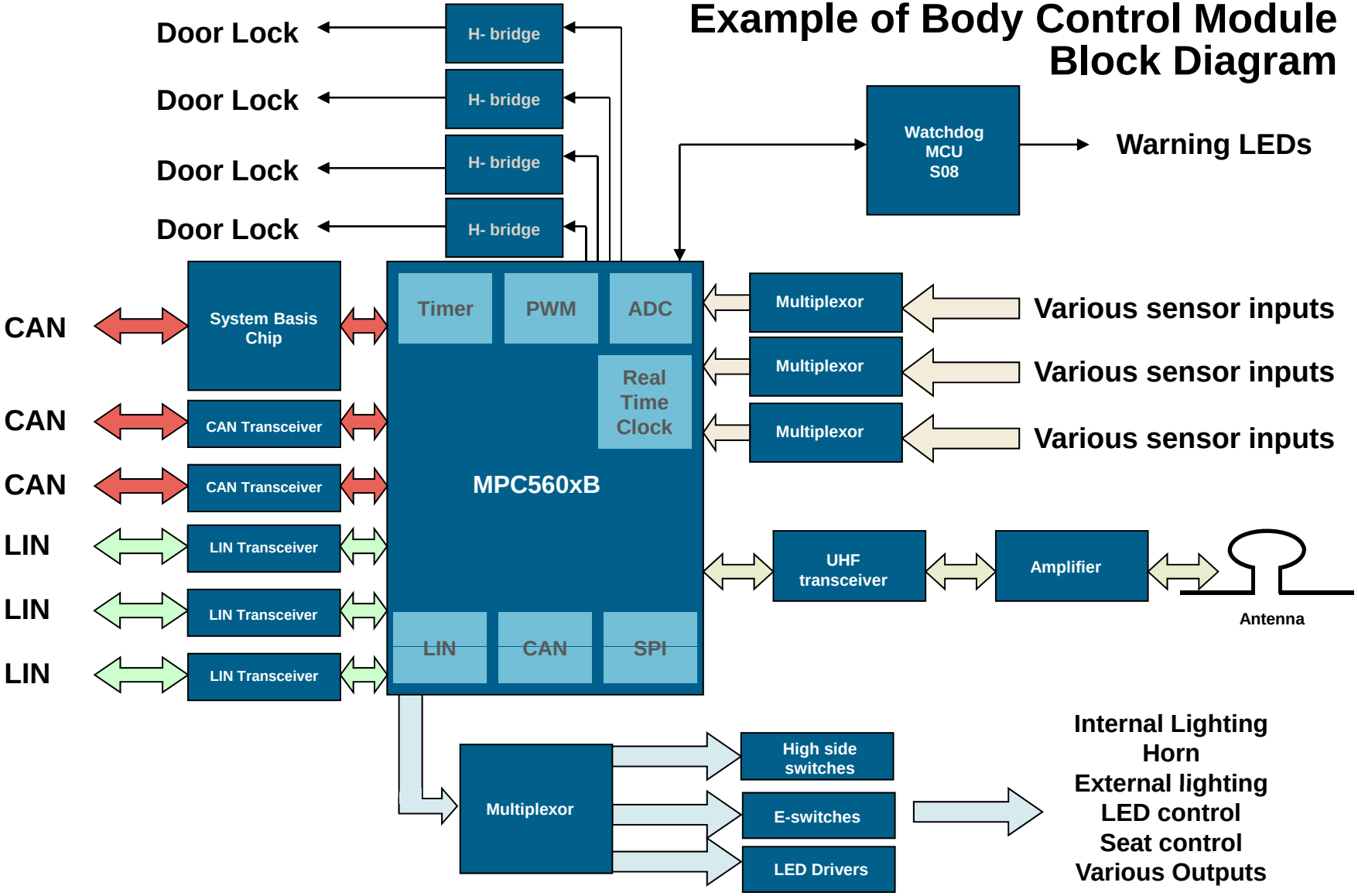
Example of Body Control Module Block Diagram



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MPC560xB/C Value Proposition

Problem	Solution
OEM's and tier 1's continually strive to integrate more features and functionality in to Body control Modules and gateways.	MPC560xB/C Family ranges from 256KB up to 1.5MB Flash and uses the same core across the product range , this enables customers to develop the application once and then reuse across a range of products platforms.
In future customers will want a bigger portfolio of Powerful microcontrollers	The MPC560xB/C is part of a bigger range of products that go from low to high end. Compatible/Scalable products will be offered in the near future that offer lower and higher memory sizes and feature sets than the MPC560xB/C.
Customers want to use the devices for a range of body controller and gateway applications.	Sophisticated peripherals: FlexCAN for CAN networking, LINFlex for LIN networking, Cross triggering units (CTU) and eMIOS provide automated buffering, cross-triggering, hence putting less constraints on software design (e.g. Lighting/ Diagnostics/EMC)
Power efficiency is key for body controllers and gateways.	Power consumption of modules increases in each generation but environmental constraints dictate that the power actually consumed must reduce. The MPC560xB/C has a number of different modes which help to save power and enable our customers to meet all known low-power requirements. This further enables platform designs.
Customers need maximum reuse and easy to use development tools.	The reuse of modules, peripherals and even the core means that the full tools ecosystem available has a huge amount of reuse across the entire MPC560xB/C family. Future family members will also be able to reuse the tools. This ensures that our customers have to expend minimizes effort required to create platform designs.
Customer demand ease of use.	Nexus2+ debug and JTAG are included on the MPC560xB/C. No cumbersome emulators, in-application code tracing can save potential costly redesigns

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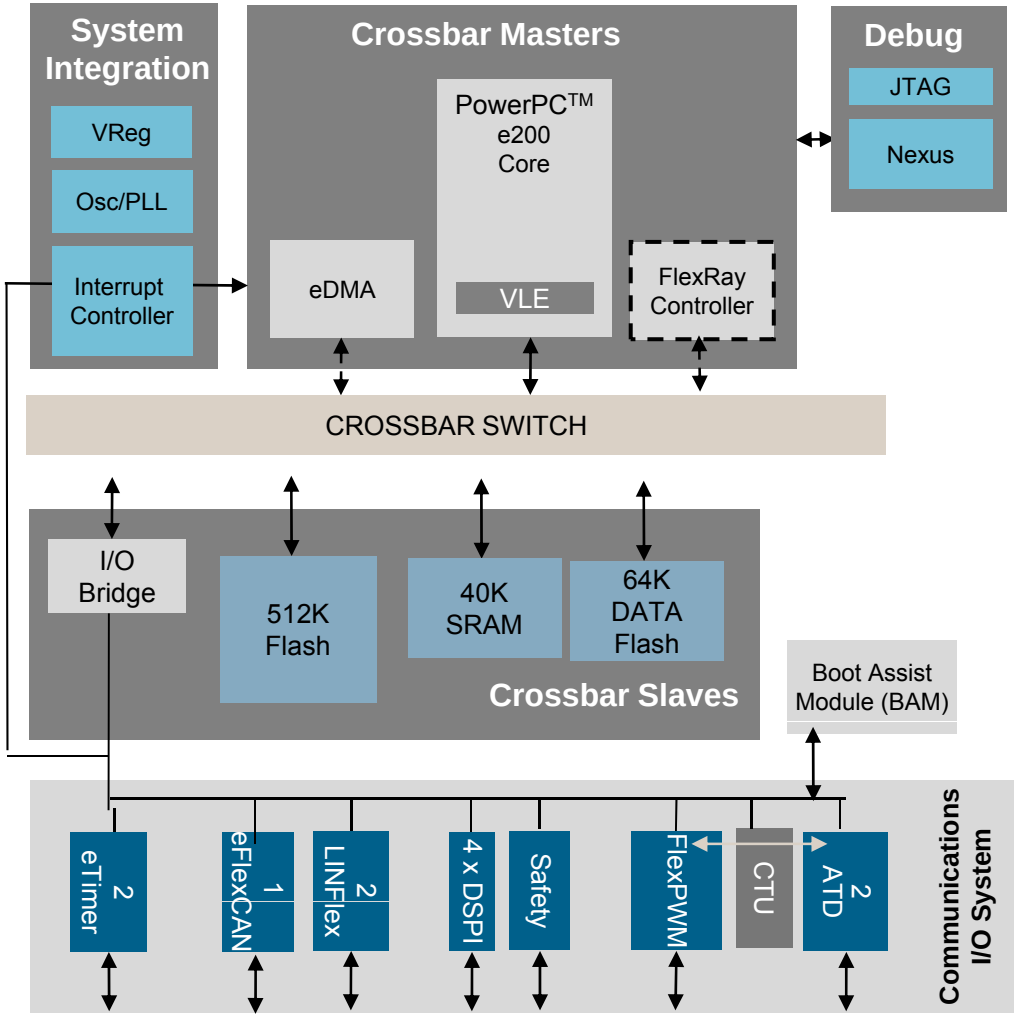
MPC5604P(Chassis & Safety)



Core
up to 64 MHz PowerPC ISA e200 zen0h core

Memory
512k byte Program Flash with ECC
4x16k byte Data Flash with ECC
40k byte SRAM with ECC

I/O
1 x FlexCAN with 32MB
1 x Safety port (can be used as additional FlexCAN - 32MB)
1 x FlexRay Dual Channel with 32MB
2 x LinFlex
4 x DSPI (4 independent chip selects each)
1 x FlexPWM (4x3 channels with 4 Fault Inputs)
1 x eTimer (6 channels incl. quad decode)
1 x eTimer (6 channels for general purpose)
2 x ADC
2x13 Ch.(4 shared channels), 10bit, conversion time <1µsec (2x8ch, 4shared on 100 pin package)
•1 x Cross-triggering unit for motor control

System
2 x PLL (one FM-PLL, one for FlexRay)
16Ch eDMA
Fault Collection Unit
16MHz internal RC OSC
Junction Temperature Sensor
JTAG / Nexus Class 2+
3.3V single supply or 5V supply with external ballast transistor
100 and 144 pins TQFP package

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Pictus - Target Applications

- Electronic power steering
- Suspension
- Braking
- Brushless DC motor
- Electric hybrid car engine
- Airbag

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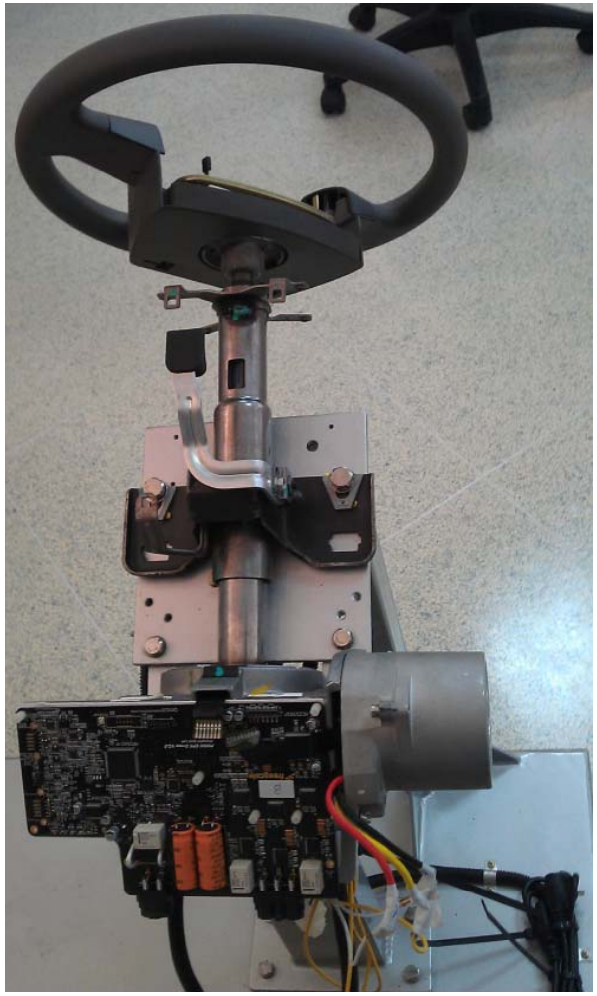
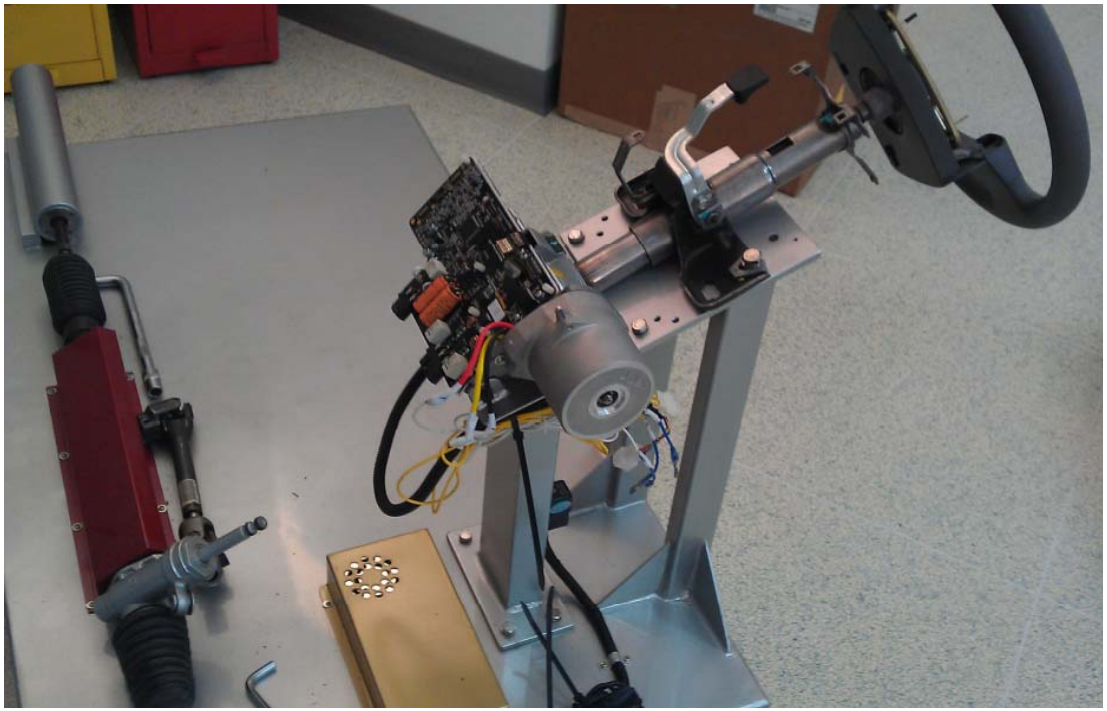
Electric Power Steering Reference Design in Shanghai Auto Lab





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Qorivva MPC560xP offers integration, performance and reliability

For industrial motor control, AC drives, and safety-critical applications. Supported by an extensive, proven ecosystem of development tools, software and design resources

Exceptional performance with high level of integration	Ideal for safety-critical applications	Faster time-to-market
Offers a rich set of real-time control peripherals with industry benchmark architecture	**Provides a series of enhanced features for accurate, reliable and robust control**	**Enabled by a proven ecosystem of development tools, software and design resources**
High-performance 64 MHz 32-bit e200z0 Power Architecture core with variable length encoding (VLE)	Hardware Error Correction Coding (ECC) on RAM and auto-grade flash memory allows memory error detection and correction	A full suite of 3rd party software and tool vendors - peripheral drivers, compilers, debuggers and RTOS's.
Up to 512KB flash and additional 64KB data flash allows for flexible, cost-efficient memory configurations depending on application needs	**Fault collection unit** (FCU) eases monitoring and management of fault events for safety-critical applications	One-click solution – development kit includes a "Getting Started" DVD with one-click access to documentation, application notes, software examples and training.
A cross triggering unit significantly reduces interrupt load due to hardware synchronization of the PWM cycle, timers and the ADCs.	Freescale market leading Automotive MCU quality and reliability with low failure rates and 15 years product longevity	
Rich set of peripherals for complex field-oriented control algorithms improves electric motor efficiency and reliability		

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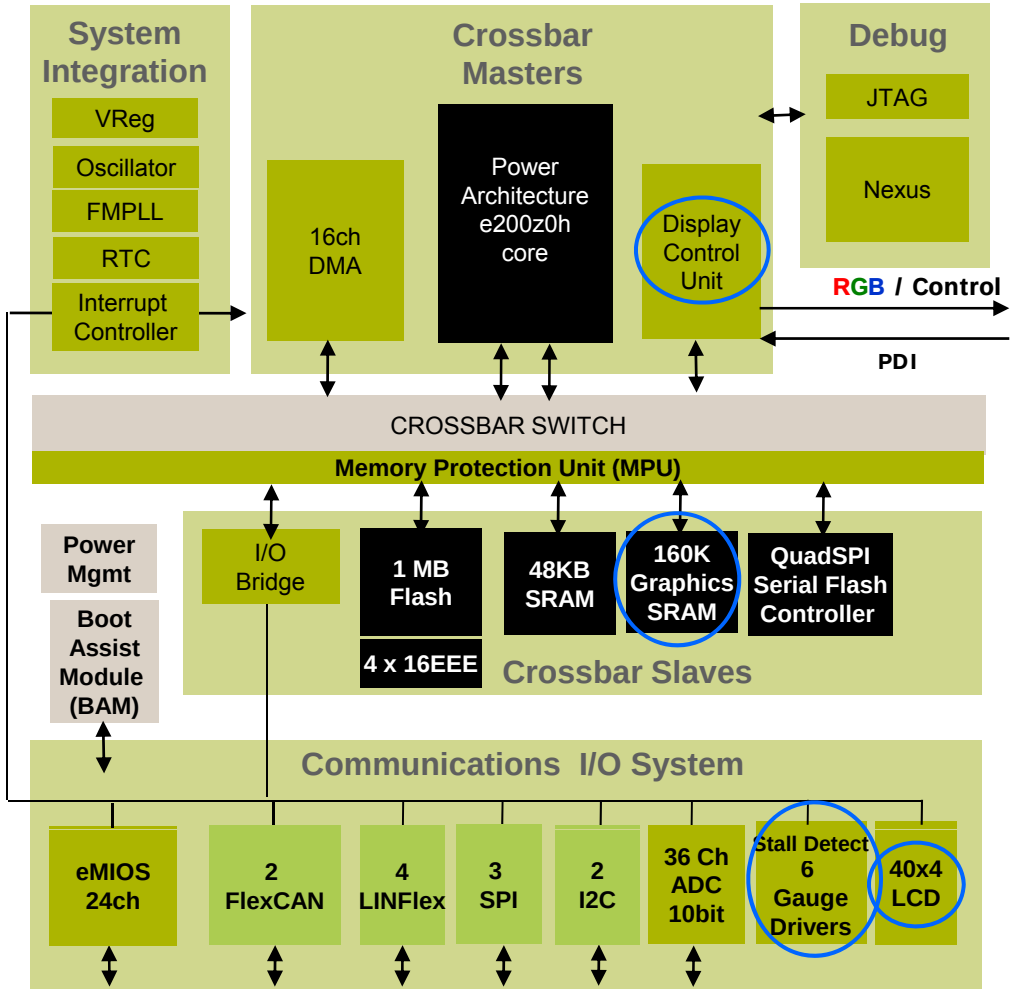
MPC560xS (Spectrum)

Family Overview

- Auto and Industrial Target Applications
  - Instrument cluster and central display applications
  - IDisplay control
- Display Control Unit
  - Enables direct drive of Quarter VGA and WQVGA.
  - Works independently of CPU to fetch, process, and display graphics data directly from multiple sources
    - Not just from Graphics RAM
    - Don't need huge (expensive) graphics RAM
  - Can move graphics data from external serial flash via QuadSPI directly into RAM for DCU too.
- SSD is key for cluster
  - Needles calibrate themselves automatically
- Low Power Design
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Multiple power domains to minimize leakage in low power modes

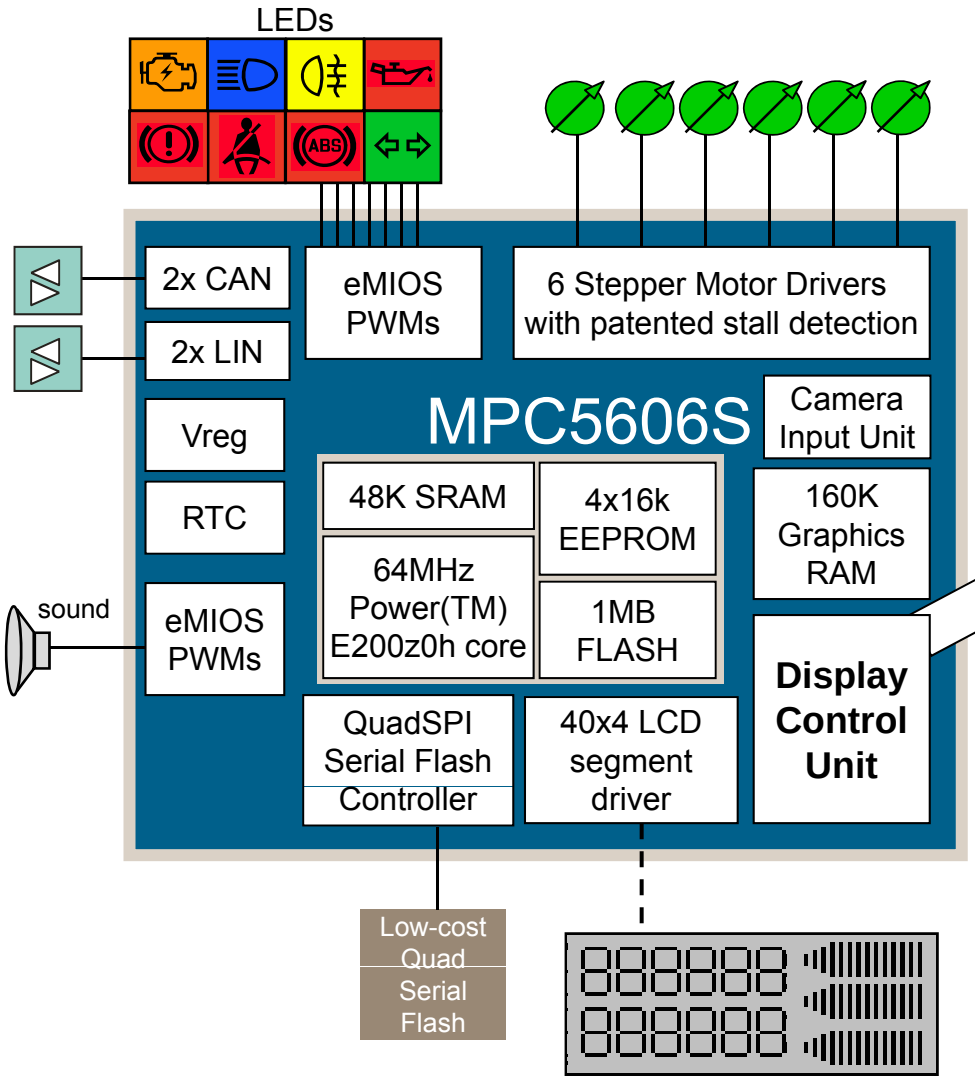


Note: block diagram represents the MPC5606S

Family Differences

Device	RAM	SRAM	TFT Drive	LCD	Mem Exp	Serial	Debug	Pins
MPC5606S	1 MB	48K SRAM + 160K Graphics RAM	Display Control Unit (DCU) with Parallel Data Interface (PDI)	40x4	QuadSPI	2xFexCAN 2xSCI 3xDSPI 4xIIC	Nexus	176, 144
MPC5604S	512 KB	48K SRAM	No	64x6	No	2xFexCAN 2xSCI 2xDSPI 2xIIC	28KB	144, 100
MPC5602S	256 KB	24K SRAM	No	64x6	No	1xFexCAN 2xSCI 3xDSPI 2xIIC	24KB	144, 100

The MPC5606S Hybrid Cluster SoC:



TFT DISPLAY

DCU on MPC5606S can drive up to 480x272 LCD with no external RAM

- Cost efficient
- Low memory requirement
- Optimized for GUI and advanced OSD
- Safety feature to enable safety related display content

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MPC5634M (Powertrain)

Core

- **40, 60, and 80MHz options Power Architecture® ISA e200z3 Core + VLE**
  - Binary User mode compatible with RCPU (MPC500) and e200z6
  - New SIMD module for DSP and floating point features

Memory

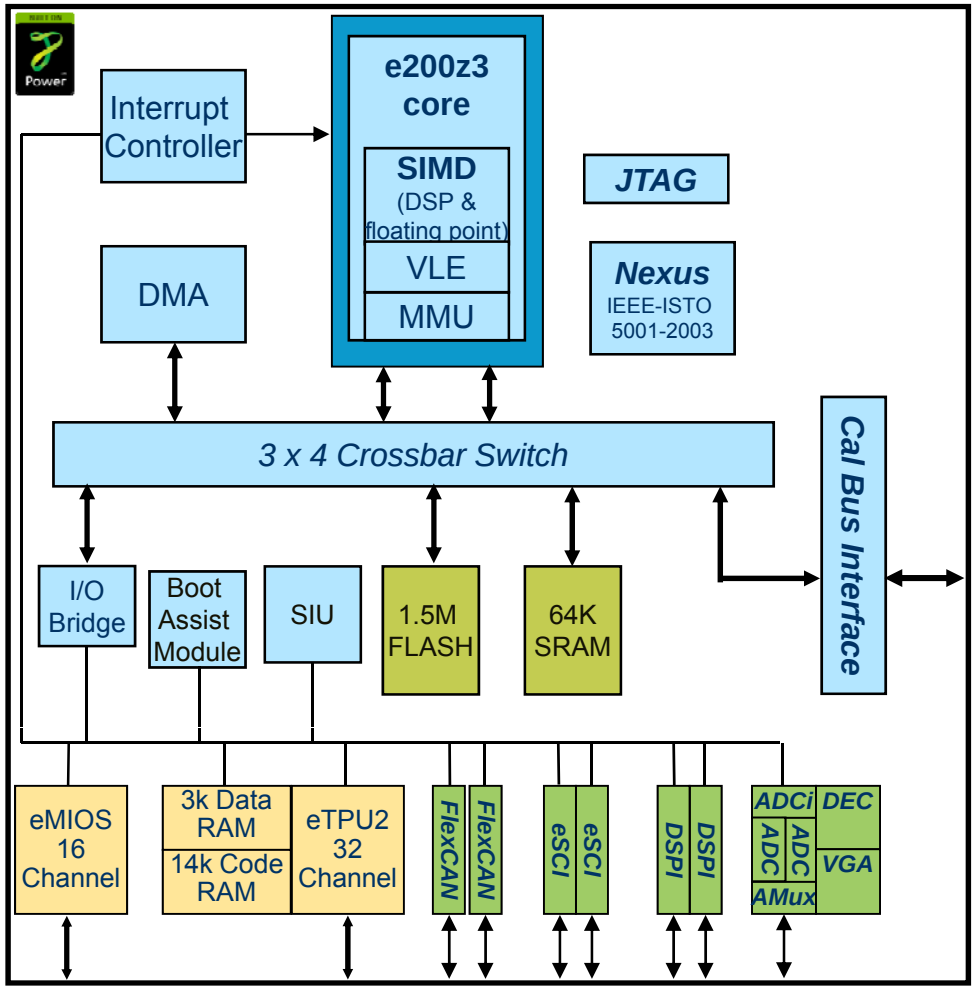
- **1.5M byte RWW Flash with ECC**
  - 81k SRAM
- **64k Data RAM (also has 32K for standby) with ECC**
  - 17k for eTPU2 (14k code & 3k parameters)

I/O

- Timed I/O Channels
- **32 channel eTPU2 + 8 additional reaction channels**
  - 16 channel eMIOS with unified channels
- 2 x FlexCAN - compatible with TouCAN, 64 + 32 buffers
  - 2 x eSCI
- 2 x DSPI 16 bits wide up to 6 chip selects each
  - Supporting Micro Second Bus
- 34 channel Dual ADC - up to 12 bit and less than 1us conversions, 6 queues with triggering and DMA support.
  - **Variable Gain Amplifier (X1, X2, X4)**
- **Decimation Filter (4th order IIR or 8th order FIR with prog.coeff.)**
  - 4 pairs differentials inputs

System

- FM-PLL
- Junction temperature sensor
- 32 Channel DMA Controller
- 196 source Interrupt Controller (plus NMI)
- Nexus IEEE-ISTO 5001-2003 Class 2+ (eTPU2 Class 1)
- **Single 5V Power supply**
- EBI for calibration (16bit, not pinned out of QFP)
- 144 LQFP package (32ADC)
- 176 LQFP package
- 208 MAPBGA (no bus, 34ADC)
- 496 CSP Vertical Calibration Bus



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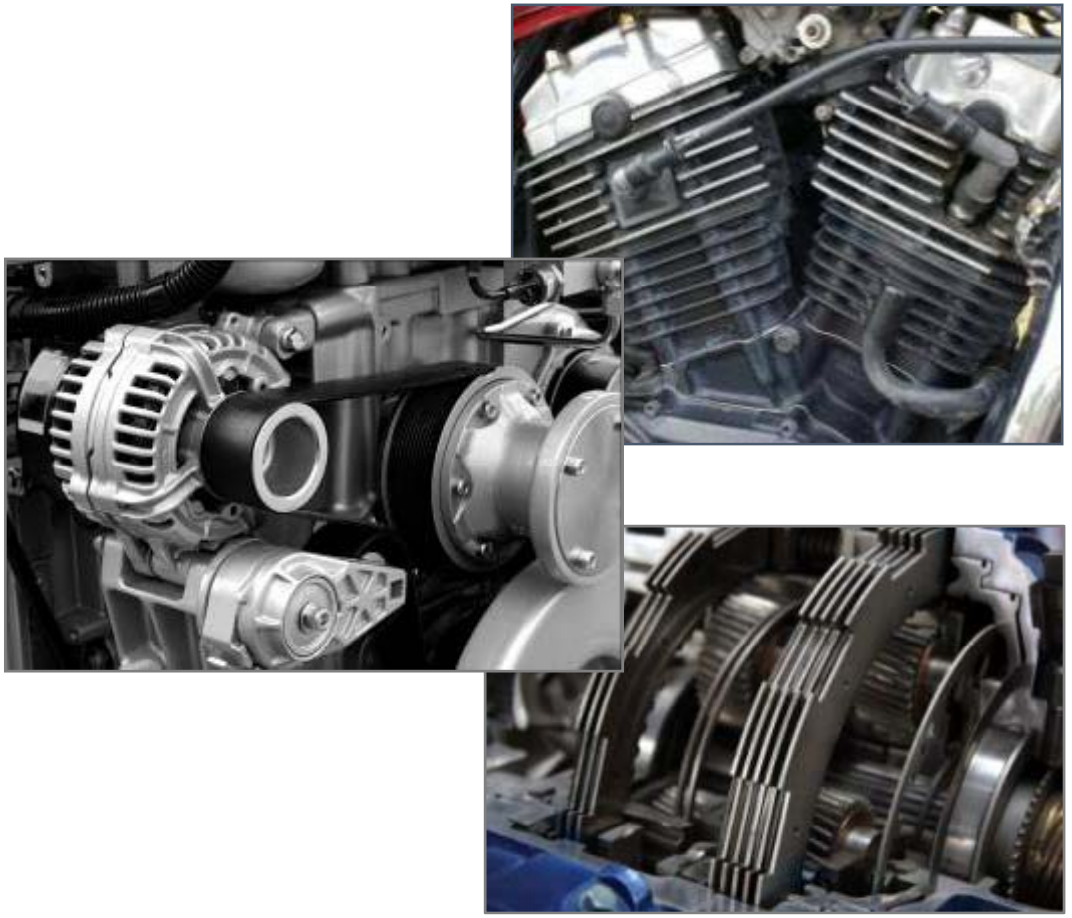
Monaco - Target Applications

- Up to 4-cylinder gasoline direct injection engines
- Entry-level diesel engines
- Entry-level transmission



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MPC563xM Key Benefits

▶Go Green by Reducing Knock

- On-chip knock system makes tight emissions controls affordable, bringing 3–5% improvement of economy and power
- Knock system helps reduce global warming by lowering CO_2 emissions by 3–5% for same amount of fuel
- Power and memory size allow fast development of “clean sheet” solutions to meet emissions legislation
- No active external components required for on-chip knock system because of variable on-chip gain and sensor bias
- Same integrated components can be used for a patented sensor diagnostics scheme that meets on-board diagnostics

▶Improves Performance

- Combination of hardware decimator and DMA can lead to a savings of up to 5% of the CPU load
- eTPU and I/O configured to handle electronic manual transmissions (paddle flap) applications where up to four brushless DC motors are used
- Offers 32 eTPU2 channels to handle complex timer applications and offload the CPU

▶Ease of Use

- Offers a 144-pin quad flat package (QFP) option; QFP has visible pins, making it easier to assemble and inspect since infrared and X-ray technology is not required
- Microsecond bus enabled for connecting ASIC with MPC563xM family

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MPC563xM Key Benefits (cont.)

- **Helps Save Cost**
  - Requires only one linear power supply (5V)
  - Compatibility with existing MPC5500 family allows code sharing and cost reduction of existing solutions into these new markets
  - No active external components are required for the on-chip knock system because variable gain and sensor bias are on-chip
  - QFP option has visible pins, making it cheaper to assemble and inspect, since infrared and X-ray technology is not required

- **Mitigates Supply Risk**
  - The MPC563xM family of devices are dual-sourced products, enabling our customers to design applications with confidence that the supply will be there

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Development Tools and Support

1.5MB Sample Part Numbers

- PPC5607BEMMGA, 208 MAPBGA
- PPC5607BEMLUA, 176 LQFP
- PPC5607BEMLQA, 144 LQFP
- PPC5607BEMLLA, 100 LQFP

512KB Sample Part Numbers

- PPC5604BEF1MMG, 208 MAPBGA
- PPC5604BEF1MLQ, 144 LQFP
- PPC5604BEF1MLL, 100 LQFP

Low Cost Demo Board

- Price: $99

Full Evaluation Kit

- Evaluation system (main module, mini module, and P&E Multilink) allow access to the CPU, all of the CPU's I/O signals, and the motherboar peripherals (such as CAN, SCI, LIN).

Type	Part#	Package supported	Suggested Resale
EVB Kit	XKT560B208SC512K	208MAPBGA	$497
EVB Kit	XKT560B144SC512K	144LQFP	$497
EVB Kit	XKT560B100SC512K	100LQFP	$497
EVB Motherboard	XPC56xxMB	--	$375
EVB Daughter Card	XDC560B208SC512K	208MAPBGA	$120
EVB Daughter Card	XDC560B144SC512K	144LQFP	$120
EVB Daughter Card	XDC560B100SC512K	100LQFP	$120
Track Board - Low Cost Starter Kit	TRK-MPC5604B	144LQFP	$99

P&E Hardware Interface Cable

- USB-ML-PPCNEXUS
- $249

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Evaluation Kit and Daughter Card Info

Evaluation Board Summary and Features

The evaluation system (motherboard and daughter card) allows full access to the CPU, all of CPU's I/O signals, and motherboard peripherals (such as CAN, SCI, LIN).

•12VDC power supply input barrel connector
• 2 CAN channels with jumper enables
• One channel with High-Speed transceiver
• One channel with Low-Speed Fault Tolerant and High-Speed transceiver (selectable with jumpers)
• 2 LIN channels with jumper enables
• One with transceiver and pin header connector populated
• One channel with footprints only
• 1 SCI channel with jumper enables
• 2 FlexRay channels with jumper enables
• One channel with transceiver and DB9 male connector
• One channel with footprint only
• 4 user push buttons with jumper enables and polarity selection
• 4 user LED's with jumper enables
• 1 potentiometer for analog voltage input

Evaluation Kit Contents

• One Motherboard
• One Daughter Card
• One XPC56xx Resources CD-ROM
• Freescale Warranty Card

Daughter Card features

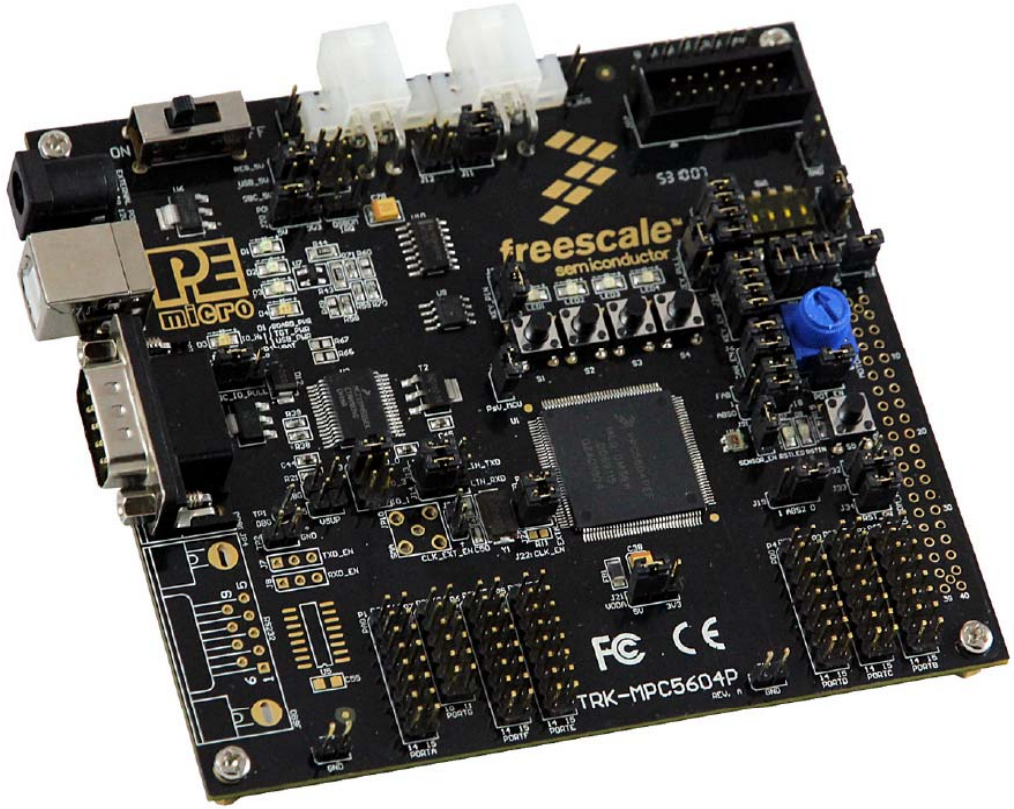
• Can be used as a stand-alone board by providing external 5V power supply input
• ON/OFF Power Switch w/ LED indicator
• Reset button with filter and LED indicator
• Debug ports: 38-pin Mictor Nexus port and/or 14-pin JTAG port
• Direct clock input through SMA connector (footprint only)
• Jumpers for boot configuration

Low Cost Evaluation Kit Info

Evaluation Board Summary and Features

The evaluation system allows full access to the CPU, all of CPU's I/O signals, and peripherals (such as CAN, SCI, LIN).

- MPC5604B/C Microcontroller in a 144LQFP package
- On-board JTAG connection via open source OSBDM circuit using the MPC9S08JM microcontroller
- MCZ3390S5EK system basis chip with advanced power management and integrated CAN transceiver
- CAN & LIN Interface
- Analog Interface with potentiometer
- High- efficiency LEDs
- SCI serial communication interface

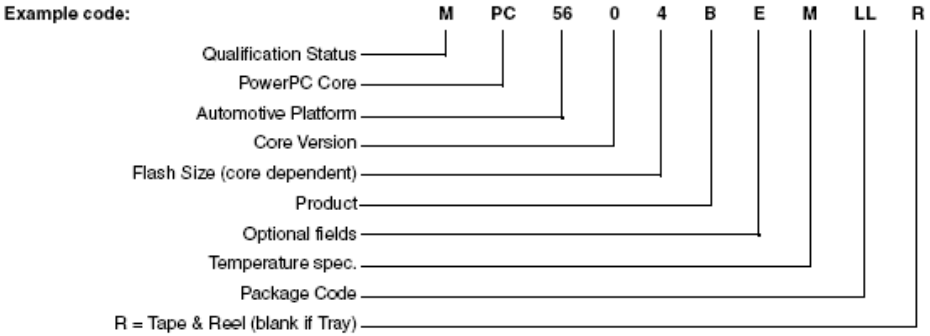


Evaluation Kit Contents

- TRK-MPC5604B Board
- TRK-MPC5604B DVD-ROM
(includes CodeWarrior software)
- USB A-to-B Cable
- Freescale Warranty Card

MPC560xB Part Number Information

MPC5604B Part # Diagram



Qualification Status
M = MC status
S = Auto qualified
P = PC status

Automotive Platform
56 = PPC in 90nm
57 = PPC in 65nm

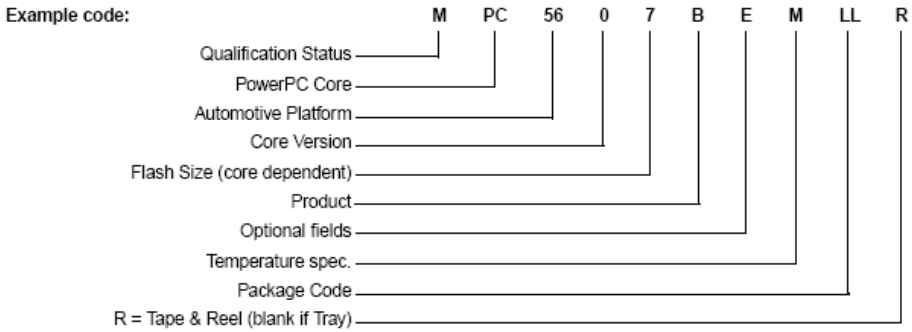
Flash Size (z0 core)
2 = 256 KB
3 = 384 KB
4 = 512 KB

Product
B = Body
C = Gateway

Temperature spec.
C = -40 to 85 °C
V = -40 to 105 °C
M = -40 to 125 °C

Package Code
LL = 100 LQFP
LQ = 144 LQFP
MG = 208 MAPBGA[1]

MPC5607B Part # Diagram



Qualification Status
M = MC status
S = Auto qualified
P = PC status

Automotive Platform
56 = PPC in 90nm
57 = PPC in 65nm

Flash Size (z0 core)
5 = 768 KB
6 = 1024 KB
7 = 1.5 MB

Product
B = Body
C = Gateway

Temperature spec.
C = –40° C to 85°C
V = –40° C to 105°C
M = –40° C to 125°C

Package Code
LL = 100 LQFP
LQ = 144 LQFP
LU= 176 LQFP

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55xx/56xx Power Architecture Tools Support

Evaluation Boards Reference Designs	freescale semiconductor; axiom MANUFACTURING SERVICES; PE micro
RTOS GUI	AUTOSAR; MCAL; Embedded Access Inc; Green Hills SOFTWARE, INC.; WIND RIVER
Compilers Simulators Debuggers	PE micro; COSMIC Software; Green Hills SOFTWARE, INC.; LAUTERBACH DEVELOPMENT TOOLS; WIND RIVER; freescale semiconductor
Stacks Drivers Translators Init Tools	freescale semiconductor; Green Hills SOFTWARE, INC.; IXXAT; WIND RIVER; mocana
eTPU Tools	freescale semiconductor; ASH www.ashware.com

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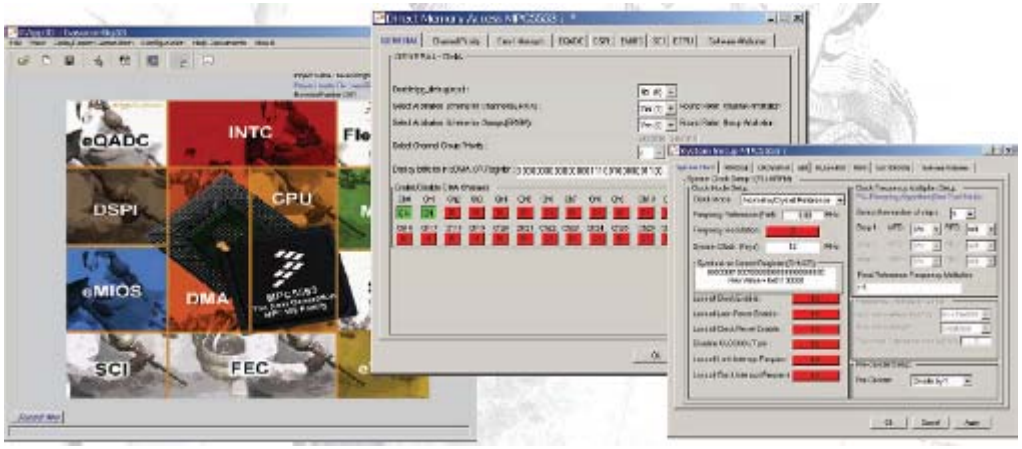
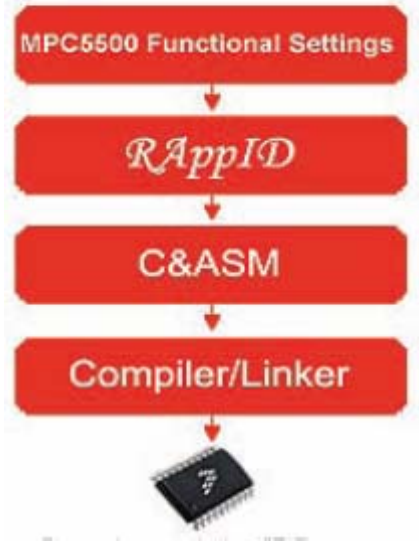
RAppID
Time to Market Improvement for the MPC560xB/C/P/M/S Family

RAppID application, initialization, and documentation software

- Comprehensive Initialization of MPC560xB/C
- GUI based tool for easy and fast development of initialization code.
- Automatic report generation of Peripheral and Register settings.
- Efficient C and Assembly code generation for a multitude of compilers like CodeWarrior™, Diab(WindRiver), and GreenHills.
- On-line documentation and built-in tool tips for ease of use
- Performs consistency checks to eliminate mistakes and inconsistencies.
- C-code and Documentation templates customizable as a service.
- Supports multiple initialization strategy code generation.





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MPC56xx Resources

MPC560xB Product Page

MPC5604BC
MPC5604B/C Data Sheet

AN2865
Example code

AN3753
MPC551x to MPC560xB/C, SPC560Bx/Cx Migration

AN3836
Advanced Headlights Control and Diagnostics

MPC5604BCRM
MPC5604B/C Microcontroller Reference Manual

E200Z0RM
e200z0 Core Reference Manual

XPC560BEVBUM
XPC560BEVB User Manual

MPC560XBCPB
MPC560xB/C Family Product Brief

EB696
New VLE Instructions for Improving Interrupt Handler Efficiency

MPC560XBFAMFS
MPC560xB Family Fact Sheet

BRFSLSFWTLAUTO
Automotive Software and Tools Brochure

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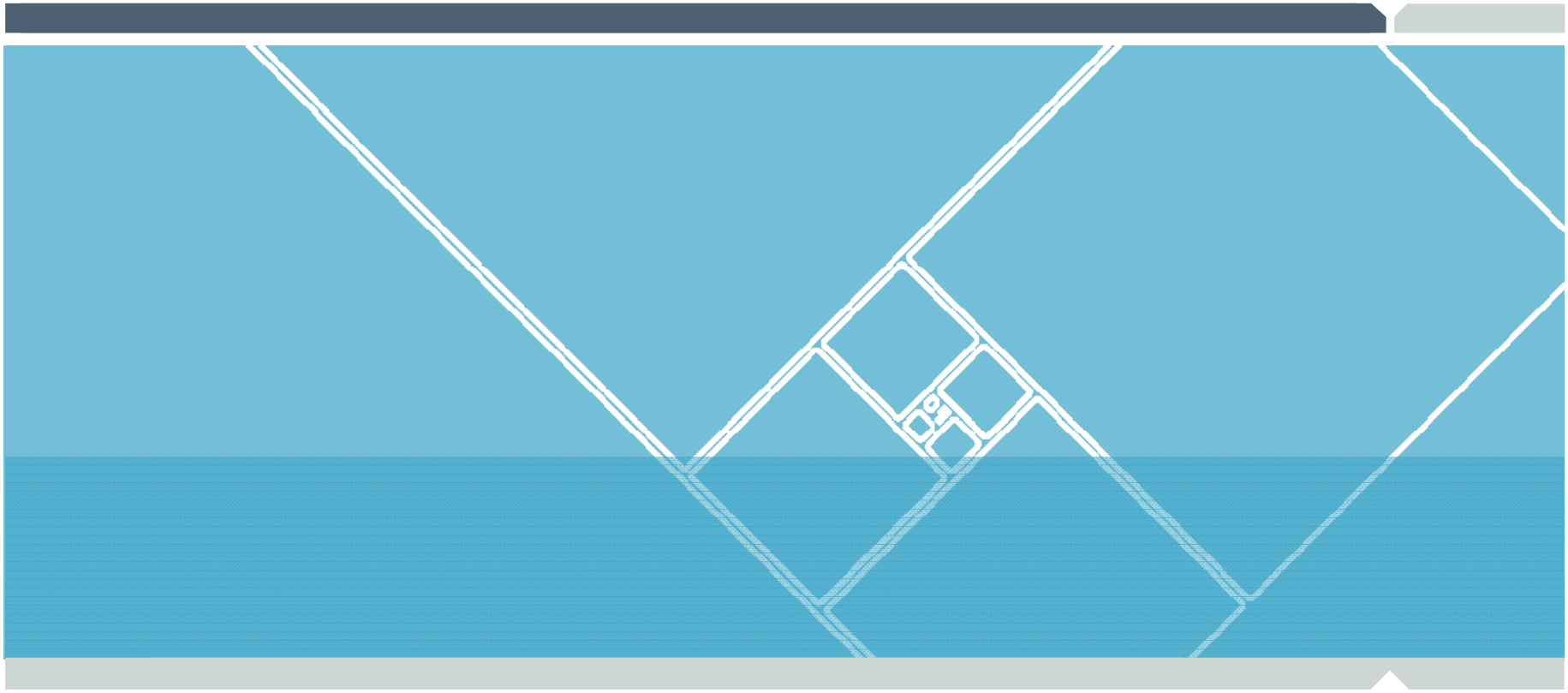
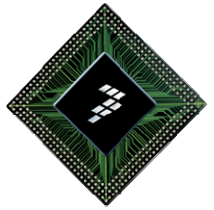


2. SIUL



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SIUL

- Introduction
- Pad Control and IOMux configuration;
- GPIO ports with data control;
- External interrupt management
- MCU Identification

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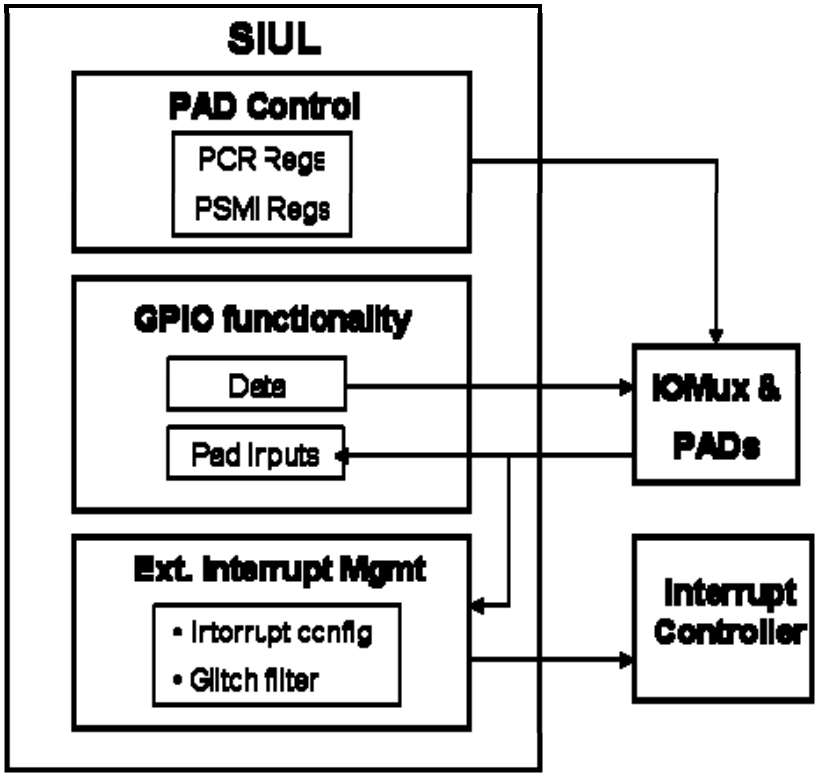
Introduction

- SIUL features the following:
- Pad Control and IOMux configuration;
  - Intended to configure the electrical parameters and mux'ing of each pad;
- GPIO ports;
  - Manages up to 123 GPIO pads organized as ports that can be accessed for data reads and writes as 32, 16 or 8-bit
- External interrupt management
  - Allows the enabling and configuration (such as filtering window, edge and mask setting) of digital glitch filters on each ext. irq;
- MCU Identification
  - Recognition of the exact MCU



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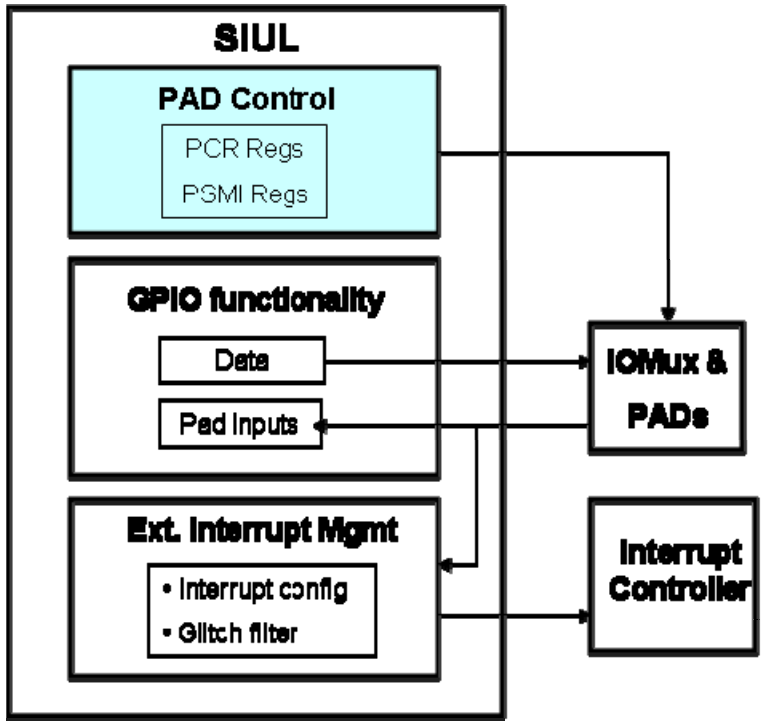
SIUL Pad Control and IOMux configuration

- Pad Control is managed through **PCR** registers

- IOMux configuration is managed through:
  - PCR Registers (output functionalities)
  - PSMI Registers (input functionalities)



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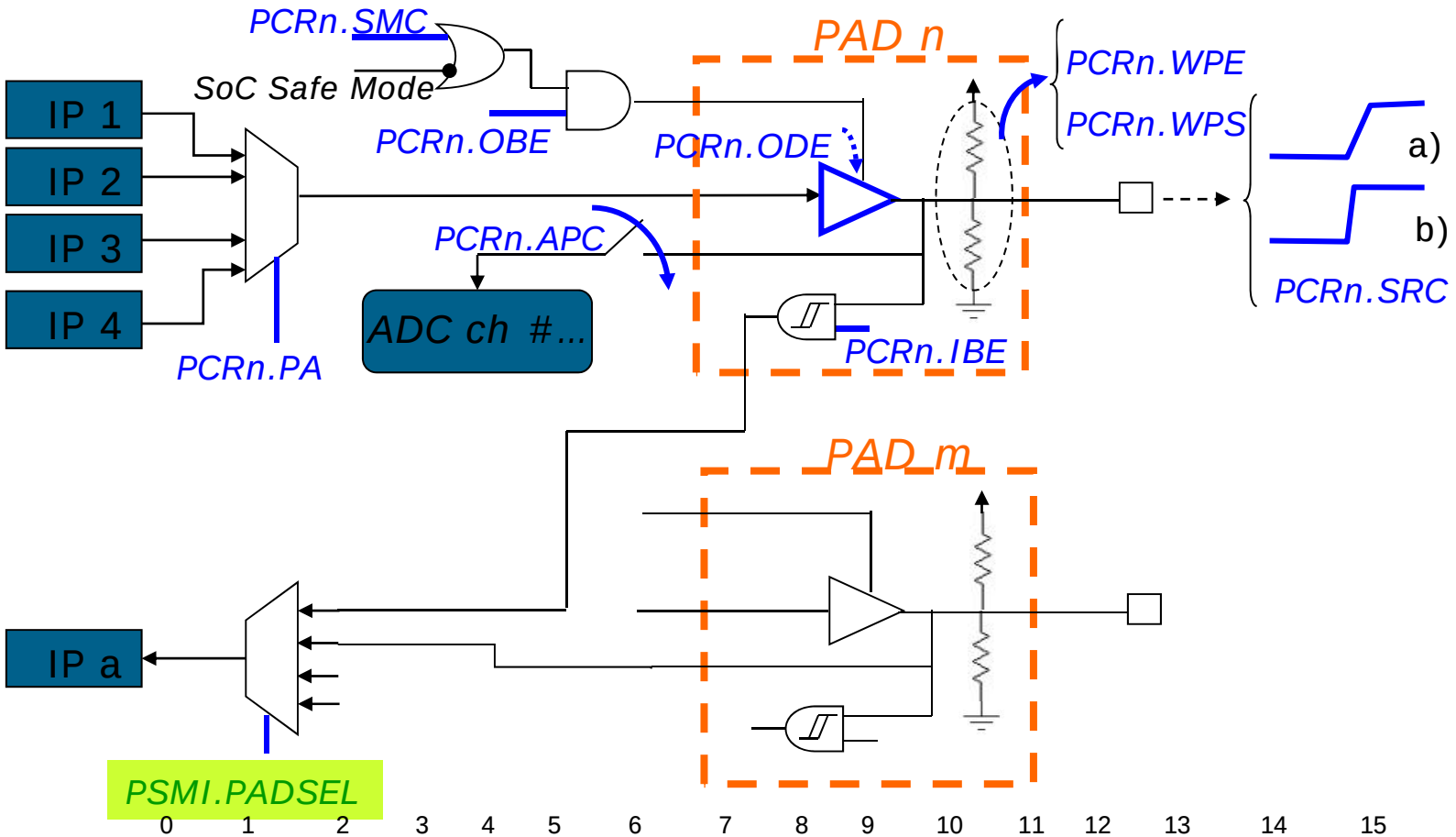
SIUL Pad Control and IOMux config



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W		SMC	APC		PA		OBE	IBE			ODE			SRC	WPE	WPS
Reset	0	0	0	0	0		0	1	0	0	0	0	0	0	0	0

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Pad Control Register (PCR) – General

- Controls configuration of the static electrical and functional characteristics associated with I/O pads
- One PCR Register per PAD
- Depending on the usage of each pad on the device, we may have:
  - PAD with GPIO and digital alternate function;
  - PAD with Slew Rate Control;
  - PAD with GPIO and analog functionality;
  - PAD dedicated to Precise ADC Channels.
- This impact the availability of certains bits in the PCR registers, as described in the following

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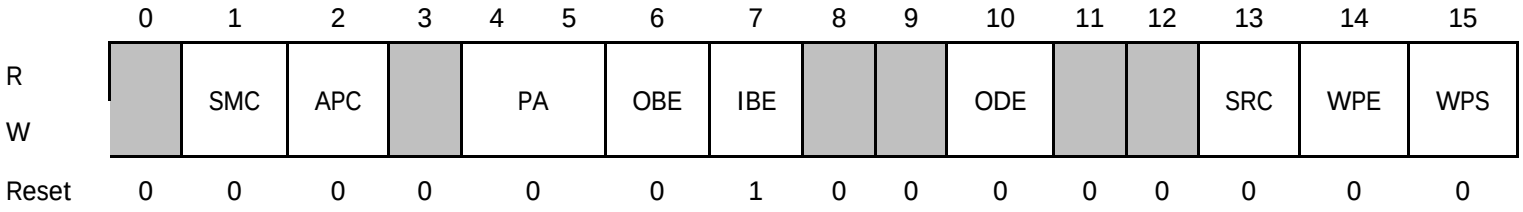
Pad Configuration Register (PCR) – Bitfields description



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W		SMC	APC		PA		OBE	IBE			ODE			SRC	WPE	WPS
Reset	0	0	0	0	0		0	1	0	0	0	0	0	0	0	0

- **SMC (Safe Mode Control):** Override automatic deactivation of the output buffer upon entering SAFE mode of the SoC.
- **APC (Analog Pad Control):** Enables the usage of the pad as analog input.
- **PA (Pad Output Assignment):** Select the function that is allowed to drive the output of a multiplexed pad.
- **OBE (Output Buffer Enable):** Enables the output buffer of the pad when in GPIO mode.
- **IBE (Input Buffer Enable):** Enables the input buffer of the pad.
- **ODE (Open Drain Output Enable):** Selects either open drain or push/pull driver configurations for the pad. This feature applies to output pads only.
- **SRC (Slew Rate Control):** Controls the slew rate of the output signals
- **WPE (Weak Pull Up/Down Enable):** Enables/Disables the weak pull up/down on the pad.
- **WPS (Weak Pull Up/Down Select):** Selects weak pull up/down if enabled.

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Peripherals
SIUL Pad Control and IOMux configuration 1/5

Alternate functions are chosen by PCR.PA bitfields:

PCR.PA = 00 -> AF0;
PCR.PA = 01 -> AF1;
PCR.PA = 10 -> AF2;
PCR.PA = 11-> AF3.

This is intended to select the output functions;

For input functions, PCR.IBE bit must be written to '1', regardless of the values selected in PCR.PA bitfields.

For this reason, the value corresponding to an input only function is reported as "--".

2.7 Functional ports A, B, C, D, E, F, G, H

The functional port pins are listed in Table 2-3.

Table 2-3. Functional Port Pin Descriptions

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type	RESET config.	Pin No. 100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[2]
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 --	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][3]	SIUL eMIOS 0 CGM eMIOS 0 WKPU	I/O I/O O I/O I	M	Tristate	12	16	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 -- --	GPIO[1] E0UC[1] - - WKUP[2](3) NMI[4]	SIUL eMIOS 0 - - WKPU WKPU	I/O I/O - - I I	S	Tristate	7	11	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 --	GPIO[2] E0UC[2] - - WKUP[3](3)	SIUL eMIOS 0 - - WKPU	I/O I/O - - I	S	Tristate	5	9	17	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 --	GPIO[3] E0UC[3] LIN5TX - EIRQ[0]	SIUL eMIOS 0 LINFlex 5 - SIUL	I/O I/O O - I	S	Tristate	68	90	114	K15

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SIUL Pad Control and IOMux config
PSMI Registers – Choosing the input pad…

	0	1	2	3	4 ... 7	8	9	10	11	12 ... 15	16	17	18	19	20 ... 23	24	25	26	27	28 ... 31
R	0	0	0	0	PADSELn	0	0	0	0	PADSEL(n+1)	0	0	0	0	PADSEL(n+2)	0	0	0	0	PADSEL(n+3)
W																				

- Different pads can be chosen as possible inputs for a certain peripheral function.
- Each PADSEL selects the pad currently used for a certain input function.

Table 15-13. Peripheral input pin selection

PSMI registers	PADSEL fields	SIUL address offset	Function / Peripheral	Mapping[1]
PSMI0_3	PADSEL0	0x500	CAN1RX / FlexCAN 1	00: PCR[35] 01: PCR[43] 10: PCR[95][2]
	PADSEL1	0x501	CAN2RX / FlexCAN 2	0: PCR[73] 1: PCR[89][2]
	PADSEL2	0x502	CAN3RX / FlexCAN 3	00: PCR[36] 01: PCR[73] 10: PCR[89][2]
	PADSEL3	0x503	CAN4RX / FlexCAN 4	00: PCR[35] 01: PCR[43] 10: PCR[95][2]

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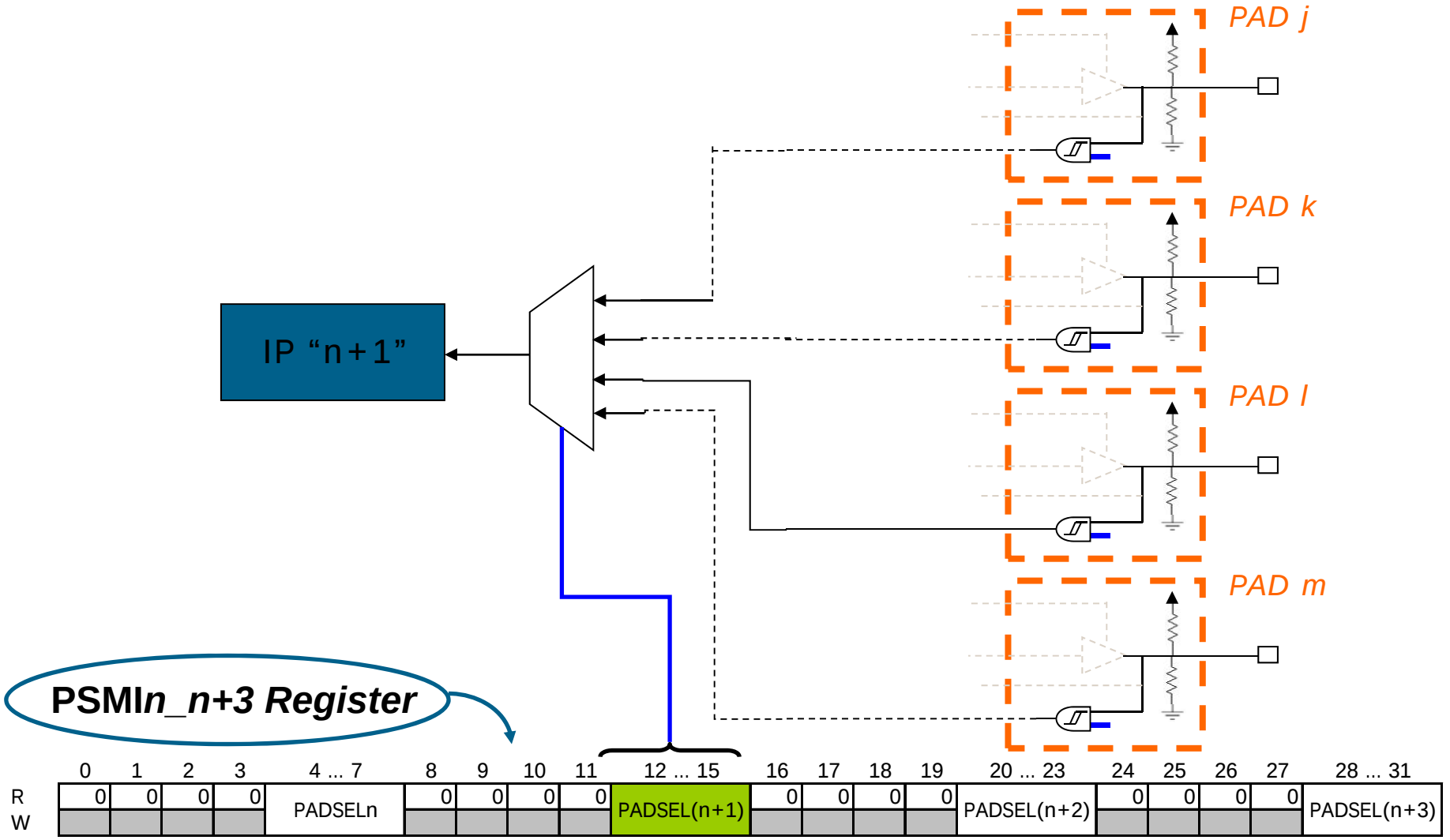
Usage of PSMI Registers – Graphic representation


PAD j
PAD k
PAD l
PAD m
IP "n+1"
PSMIn_n+3 Register
0 1 2 3 4 ... 7 8 9 10 11 12 ... 15 16 17 18 19 20 ... 23 24 25 26 27 28 ... 31
R
W
0 0 0 0 PADSELn 0 0 0 0 PADSEL(n+1) 0 0 0 0 PADSEL(n+2) 0 0 0 0 PADSEL(n+3)

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SIUL GPIO Functionality

- SIUL manages/accesses GPIO pads both:
  - On individual base (R/W access to a single GPIO);
    - Access is done on a byte basis
  - On port base (parallel access).

- Ports accesses can be:
  - Data Read: 32-bit, 16-bit or 8-bit accesses
  - Data Write: 32-bit (only if not masked access), 16-bit or 8-bit

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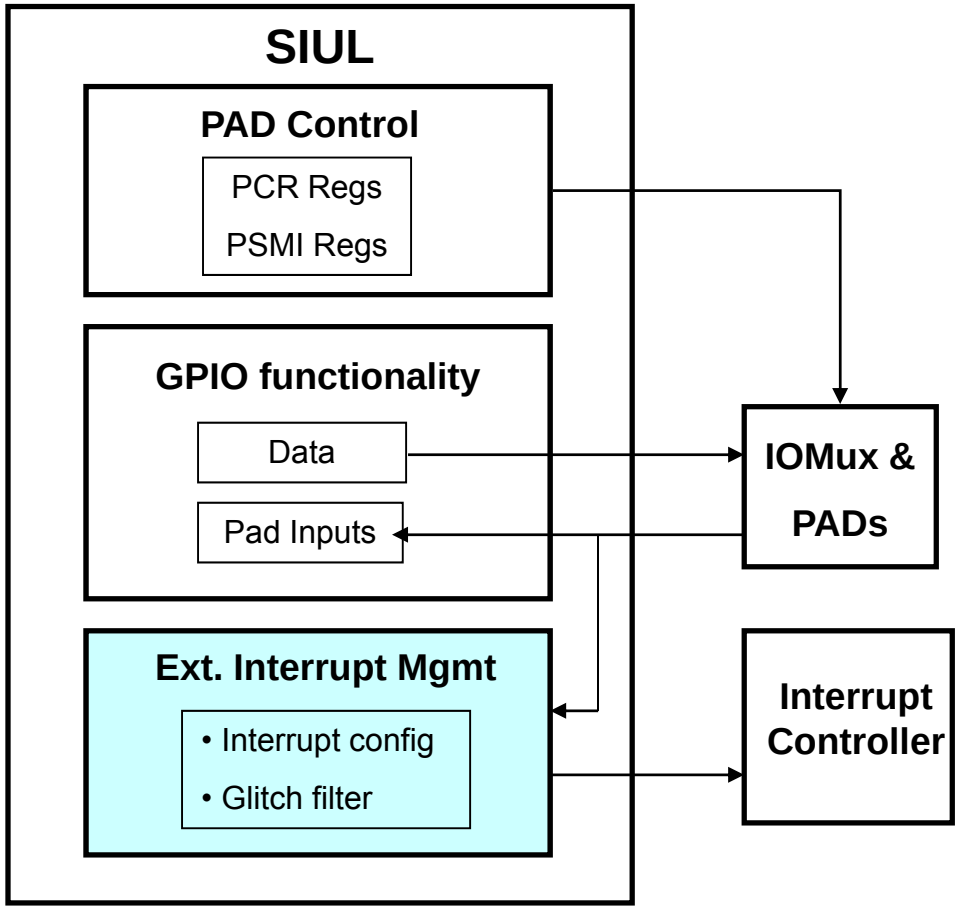
SIUL External Interrupt Management



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SIUL MCU Identification Registers (MDIR)

- SIUL includes two registers that can be read by users and tools manufactures to determine what device is present (which part number, pkg, flash size etc.) and to take the corresponding actions. These registers are called:

  - MIDR1

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	Part No																CSP	PKG					0	0	Mask_No_Major				Mask_No_ Minor			
W																																

  - MIDR2

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	S/F	Flash_Size_1				Flash_Size_2				0	0	0	0	0	0	0	Part_No								0	0	0	EE	0	0	0	FR
W																																

    - FR bit is at ‘0’ for Bolero

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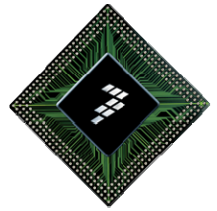

3. System Clock Module / Timer

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CGM Clock sources

- Main Clock
  - 4-16 MHz External Crystal/Oscillator -> FXOSC
  - 16 MHz Internal RC Oscillator -> IRC
    - Default system clock at reset output (DRUN mode)
    - Trimble
- Low Power Clock
  - 32 kHz External Crystal/Oscillator -> OSC_32k
    - Low power oscillator
    - Dedicated for RTC/API
  - 128 kHz Internal RC Oscillator
    - Dedicated for RTC/API and watchdog
    - Optional clock for LCD driver in STANDBY modes
    - Trimble

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CGM PLLs

- FMPLL clocked by FXOSC
  - Optional output clock frequency modulation for current consumption spreading
  - Optionally monitored by CMU
  - can be used as system clock

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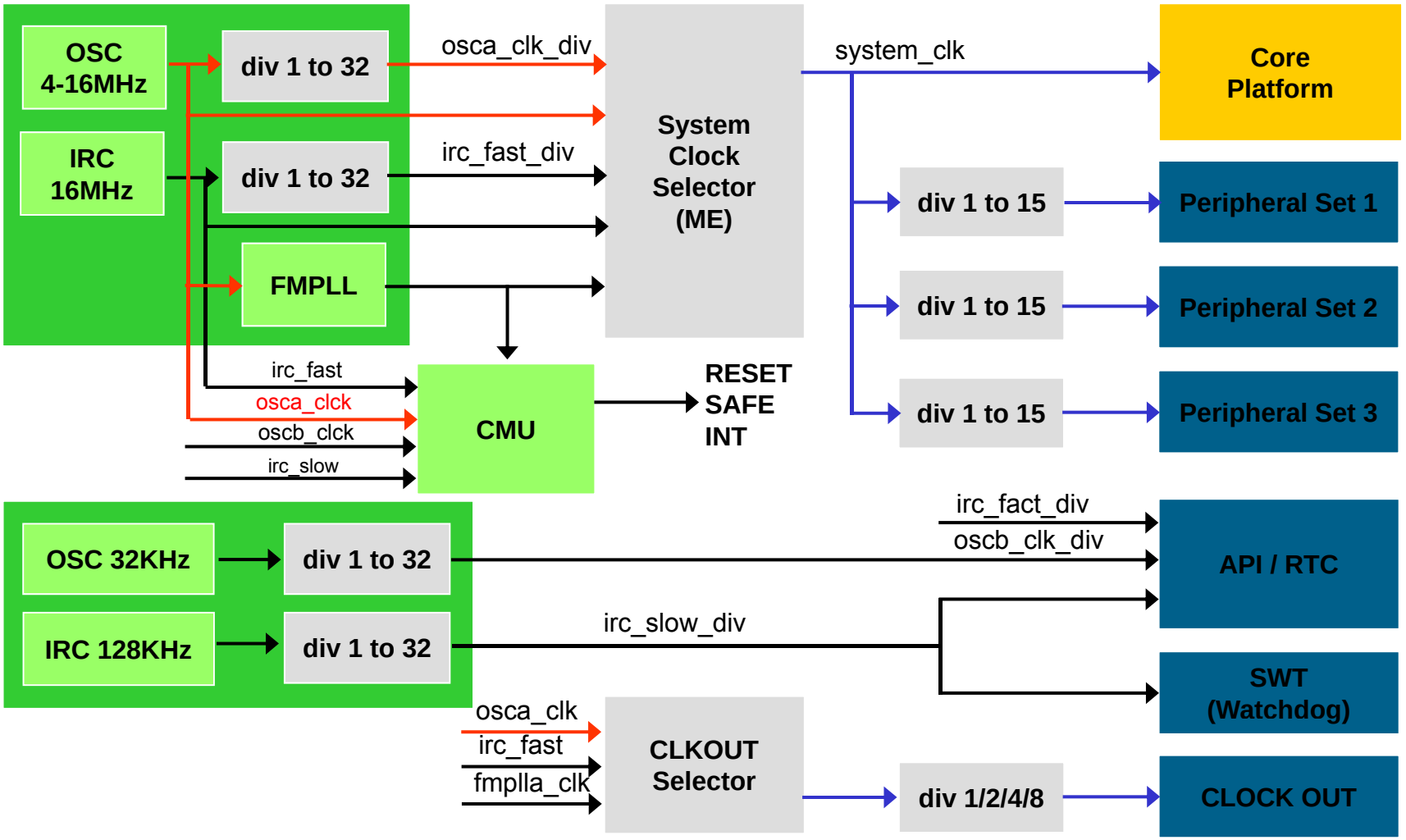
CGM Clocking Structure



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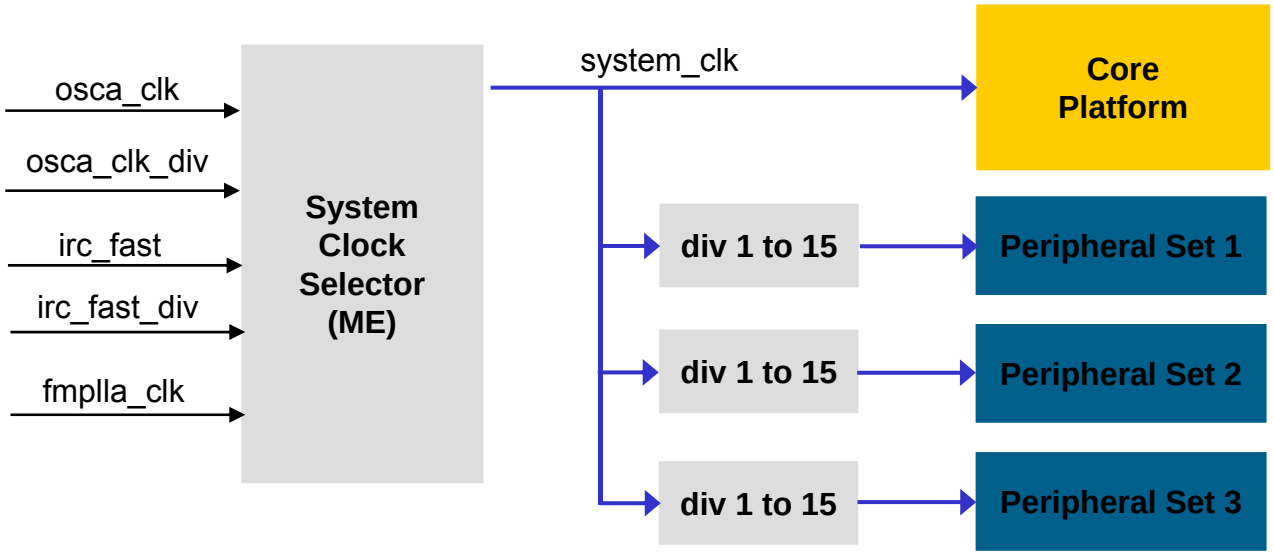
CGM System Clock Description

- Provides the clock (divided or not) to the Core/Peripherals
- Selected by ME_XXX_MC register



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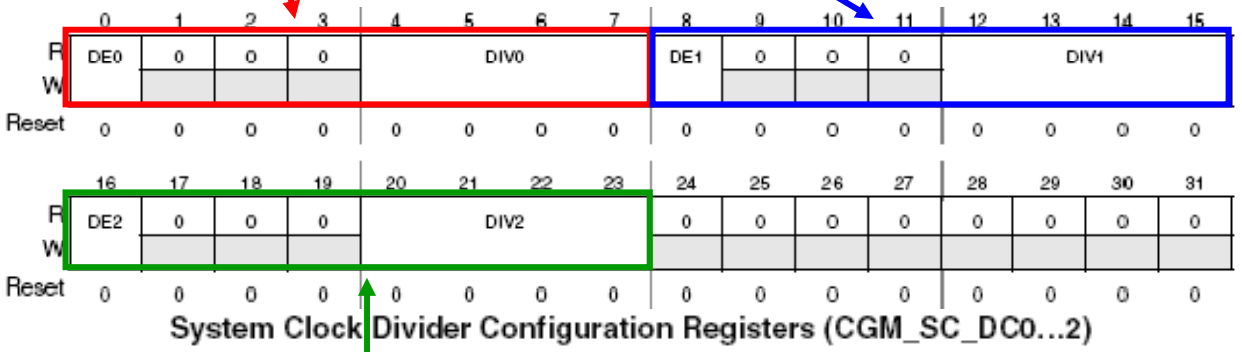
Peripheral Set Divider Configuration Register

▶Peripheral Set 1	▶Peripheral Set 2	▶Peripheral Set 3
▶All LINFlex modules	▶All FlexCAN modules	▶All eMIOS modules
▶All I2C modules	▶All DSPI modules	▶CTU
		▶ADC



System Clock Divider Configuration Registers (CGM_SC_DC0...2)

DEx: Peripheral Set x Divider Enable
DIVx: Peripheral Set x Divider x Division Value (1..16)

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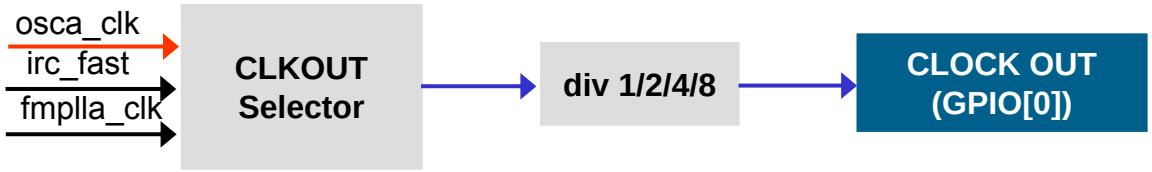
CGM Output Clock

- Clock output on the GPIO[0] pin



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	SELDIV		SELCTL				0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Output Clock Division Select Register (CGM_OCDS_SC)

SELDIV:	division by 1,2,4,8
SELCTL:	clock source (OscA, Irc fast, pll) selection

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CGM Source Clock Main Feature Summary

	Division factors range from 1,2,3…32	Trimble	Signaling status in STANDBY Mode	Switching on/off controlled by Mode Entry	Bypass mode	Clock available interrupt	Configurable start-up time
FXOSC 4-16MHz	Yes	N/A	Yes	Yes	Yes	Yes	Yes
SXOSC 32K	Yes	N/A	Yes	Yes	Yes	Yes	Yes
FIRC 16MHz	Yes	(+/- 1%)	Yes	Yes	No	No	No
SIRC 128K	Yes	(+/- 1%)	Yes	*	No	No	No

*Note: Control SIRC_128K state (ON/OFF) in only availabel in STANDBY Mode. In all other modes e.g. RUN, HALT, the SIRC is always ON

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FMPLL

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CGM Frequency Modulated PLL (FMPLL)

- The purpose of the FMPLL is to generate a 64 MHz (max) system clock from the FXOSC.
- The FMPLL operating modes:
  - Power down
  - Progressive clock switching
  - Normal
  - Normal with frequency modulation to reduce EMC
- These modes are controlled by two registers:
  - Control Register (CR)
  - Modulation Register (MR)

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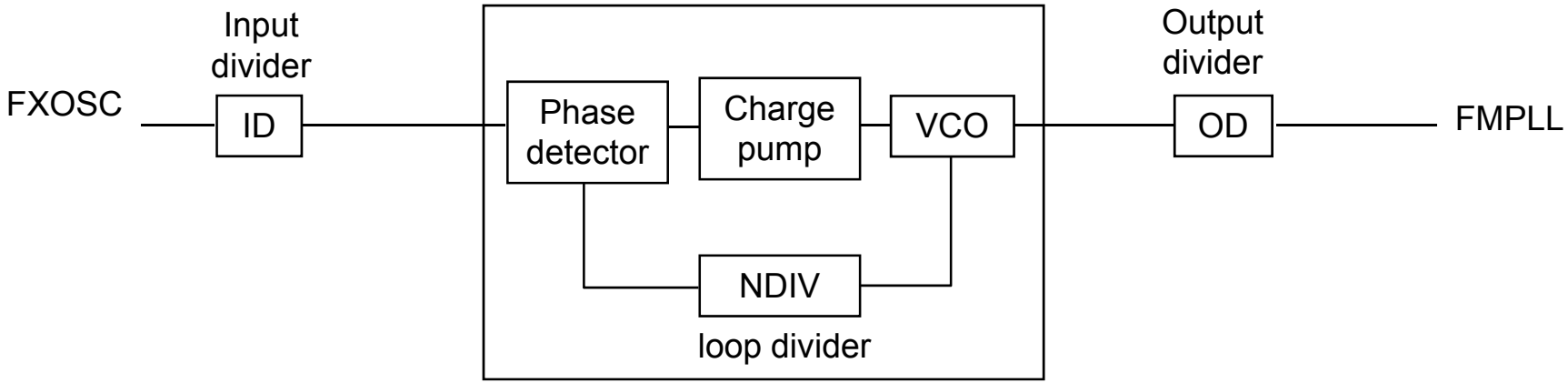
CGM FMPLL
Normal mode

- The PLL output clock frequency derives from the relation:
-
-

$$FMPLL = (FXOSC \times NDIV) / (IDF \times ODF)$$



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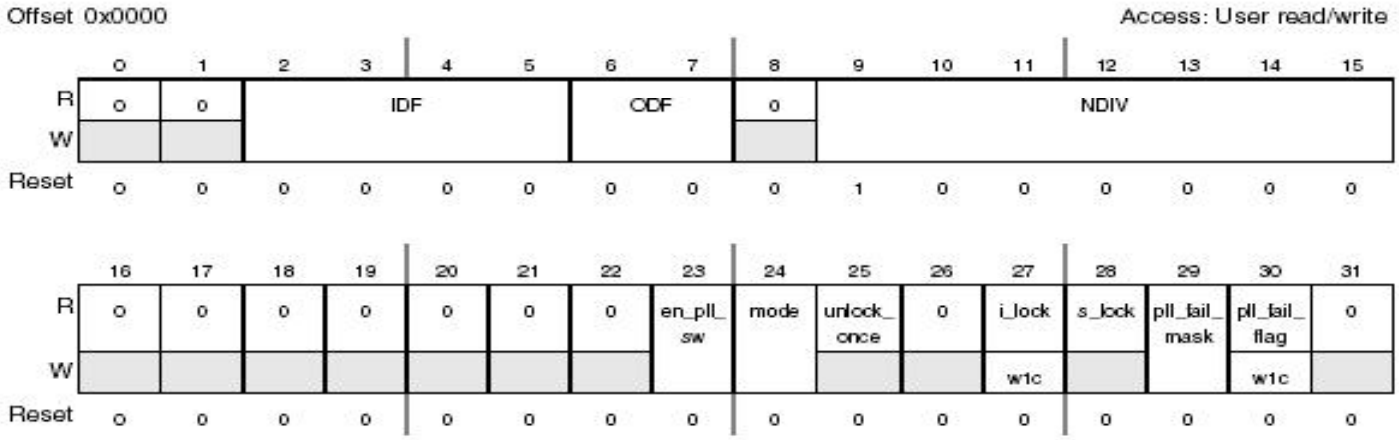
CGM FMPLL Control Register (CR) 1/2


Offset 0x0000
Access: User read/write
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
R 0 0 IDF ODF 0 NDIV
W
Reset 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
R 0 0 0 0 0 0 0 en_pll_sw mode unlock_once 0 i_lock s_lock pll_fail_mask pll_fail_flag 0
W w1c w1c
Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Bit name	Bit description
2-5	IDF	The value of this field sets the PLL Input division factor.
6-7	ODF	The value of this field sets the PLL Output division factor
9-15	NDIV	The value of this field sets the PLL Loop division factor

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CGM FMPLL Control Register (CR) 2/2

Bit	Bit name	Bit description
23	en_pll_sw	This bit is used to enable progressive clock switching.
24	mode	This bit is used to activate the 1:1 Mode.
25	unlock_once	This bit is a sticky indication of PLL loss of lock condition. Unlock_once is set when the PLL loses lock. Whenever the PLL reacquires lock, unlock_once remains set. Only por_rst_b can clear this bit.
27	i_lock	This bit is set by hardware whenever there is a lock/unlock event.It is cleared by software, writing 1.
28	s_lock	This bit is an indication of whether the PLL has acquired lock.
29	pll_fail_mask	This bit is used to mask the pll_fail output.
30	pll_fail_flag	This bit is asynchronously set by hardware whenever a loss of lock event occurs while PLL is switched on. It is cleared by software, writing 1.

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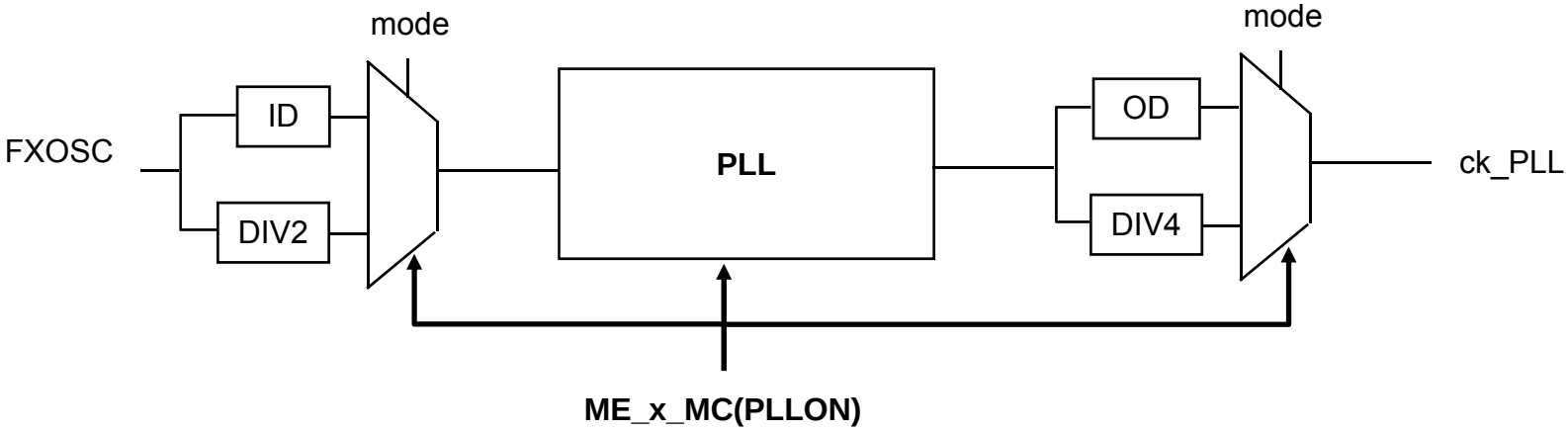
CGM FMPLL Power down mode

- The power down mode is controlled by the PLLON bit in every Mode Entry mode configuration registers (ME_x_MC). In this mode, the PLL reach its lowest current consumption and of course does not provide any clock.



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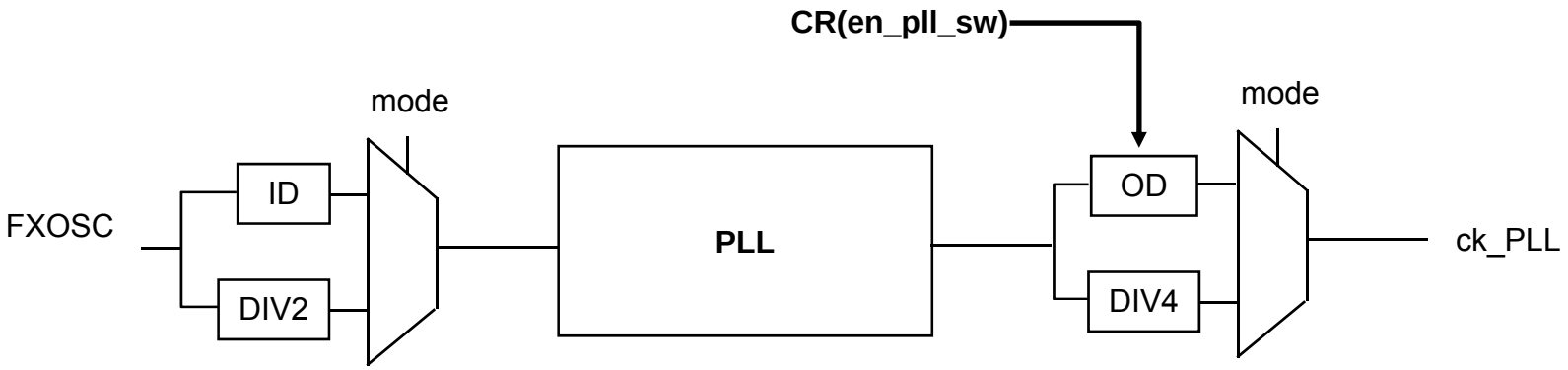
CGM FMPLL Progressive clock switching mode

- Progressive clock switching allows to switch FXOSC input clock to PLL output clock stepping through different division factors:

  This means that the current consumption gradually increases and so the voltage regulator has a better response.

- This mode is enabled by setting bit PLL_CR(en_pll_sw), and then enabling the PLL by setting the bit ME_x_MC(PLLON).



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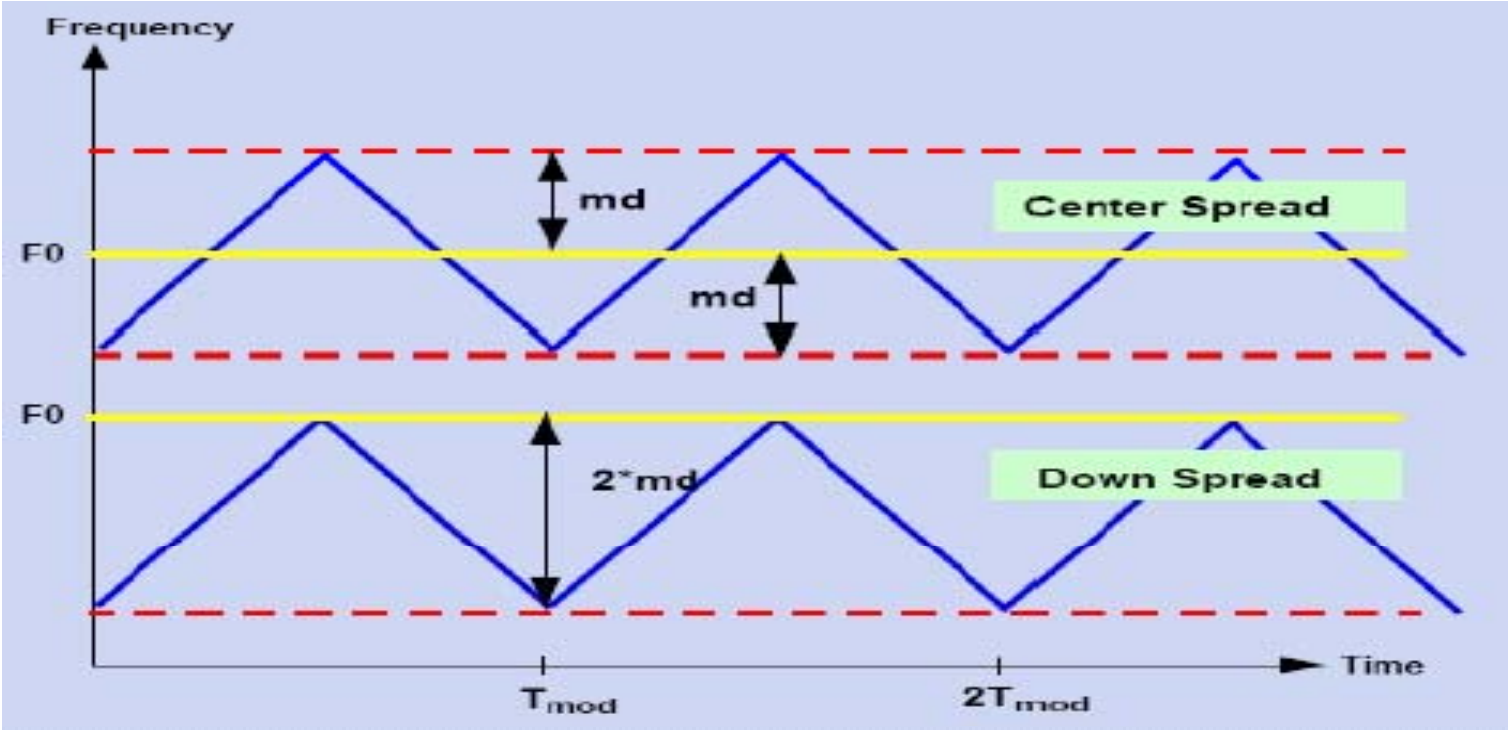
FMPLL: Normal mode + frequency modulation 1/3



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Clock Monitor Unit (CMU)

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CGM Clock Monitoring Unit (CMU)

- PLL clock monitoring : Detect if PLL leaves an upper or lower frequency boundary in turn can then switch to a SAFE mode.
- Crystal clock monitoring : Monitor the external crystal oscillator clock which must be greater than the internal RC clock divided by a division factor given by RCDIV[1:0] of CMU_CSR register. Also in turn can then switch to a SAFE mode.
- Frequency meter : measure the frequency of a internal RC versus a known reference clock XOSC

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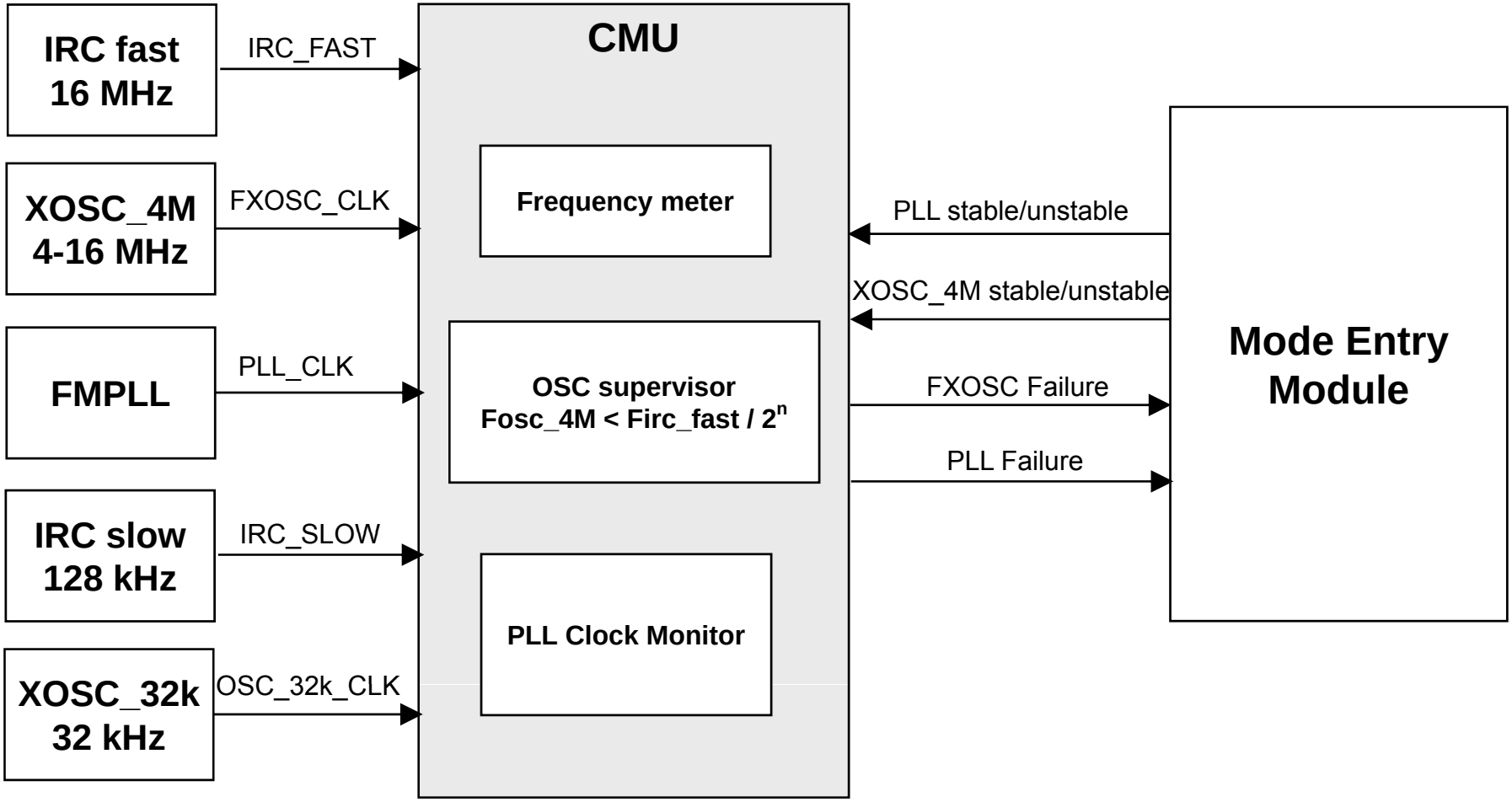
CGM CMU Block Diagram



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Timer

STM
RTC (API)
SWT
PIT

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Timer

Attributes / Timer	Clock Source	Features/Functions	Application
STM	System clock	❖ 8-bit prescaler,1~256 ❖ 32-bit wide ❖ 1 up counter ❖ 4 cmp channels with separate interrupt source for each	Common system and application timing
PIT	System clock	❖ no internal prescaler ❖ 6-channel with 32-bit width ❖ generate periodic interrupt ❖ generate DMA trigger pulse, can trigger ADC conversion	Common system and application timing
RTC (API)	System clock	❖ 3 selectable clock source: — SIRC (128 kHz) — SXOSC (32 kHz) — FIRC (16 MHz) ❖ optional 512 and 32 prescaler ❖ autonomous periodical interrupt ❖ RTC status/control register are reset only by POR	Free running counter for time keeping applications. Runs in all modes of operation.
SWT	SIRC-128kHz	❖ no internal prescaler ❖ 32-bit counter ❖ optionally run in debug and stop mode, but not available in standby mode ❖ regular or window mode serive	watchdog

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Real Time Counter (RTC)

3 selectable counter clock sources
- SIRC128K
- SXOSC32K
- FIRC16M

Optional 512 prescaler and optional 32 prescaler
32-bit counter
- supports times up to 1.5 months with 1 ms resolution
- runs in all modes of operation
- reset when disabled by software and by POR

2-bit compare value
to support interrupt intervals of 1s up to greater than 1 hr with 1s resolution

RTC compare value changeable while counter is running
RTC status and control register are reset only by POR

Autonomous periodic interrupt (API)

10-bit compare value to support wakeup intervals of 1.0 ms to 1 s
compare value changeable while counter is running

Configurable interrupt for RTC match, API match, and RTC rollover

Configurable wakeup event for RTC match, API match, and RTC rollover

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PIT timer Module

Periodic Interrupt Timer (PIT) features:

32-bit counter resolution
clocked by system clock
timer can generate interrupt
independent timeout periods for each timer
Channel outputs can trigger ADC conversion
MPC5602/3/4 -> 6 PITs

PIT Nr.	Interrupt	Peripheral Trigger	DMA Trigger
0	YES	NO	YES
1	YES	NO	YES
2	YES	10-bit ADC	NO
3	YES	BCTU ch28	NO
4	YES	NO	YES
5	YES	NO	YES

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Watchdog Introduction

Watchdog is used to provide a system error recovery function, e.g. from software loop traps or failing bus transaction

Software must periodically write a servicing sequence prior to the next expiration of the watchdog timer interval to avoid reset or interrupt by watchdog

Writing the sequence resets the timer to the specified time-out period

Programmable selection of window mode or regular servicing

The MPC560xB watchdog resides in the Safety Module

Watchdog is default enabled

- Default : Watchdog is enabled
- Can be disabled by default by programming WATCHDOG_EN Bit in NVUSRO Register Bit 31in Shadow Flash

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Watchdog Feature List

32-bit time-out register to set the time-out period

The SWT counter clock is the undivided clock provided by internal safe clock (128KHz oscillator), no other clock source can be selected

The Watchdog can be configured to generate a reset or interrupt on an initial time-out, it will always generate a reset on consecutive time-outs

Programmable selection of window mode or regular servicing

Hard-lock (by reset) and soft-lock (by software) of configuration

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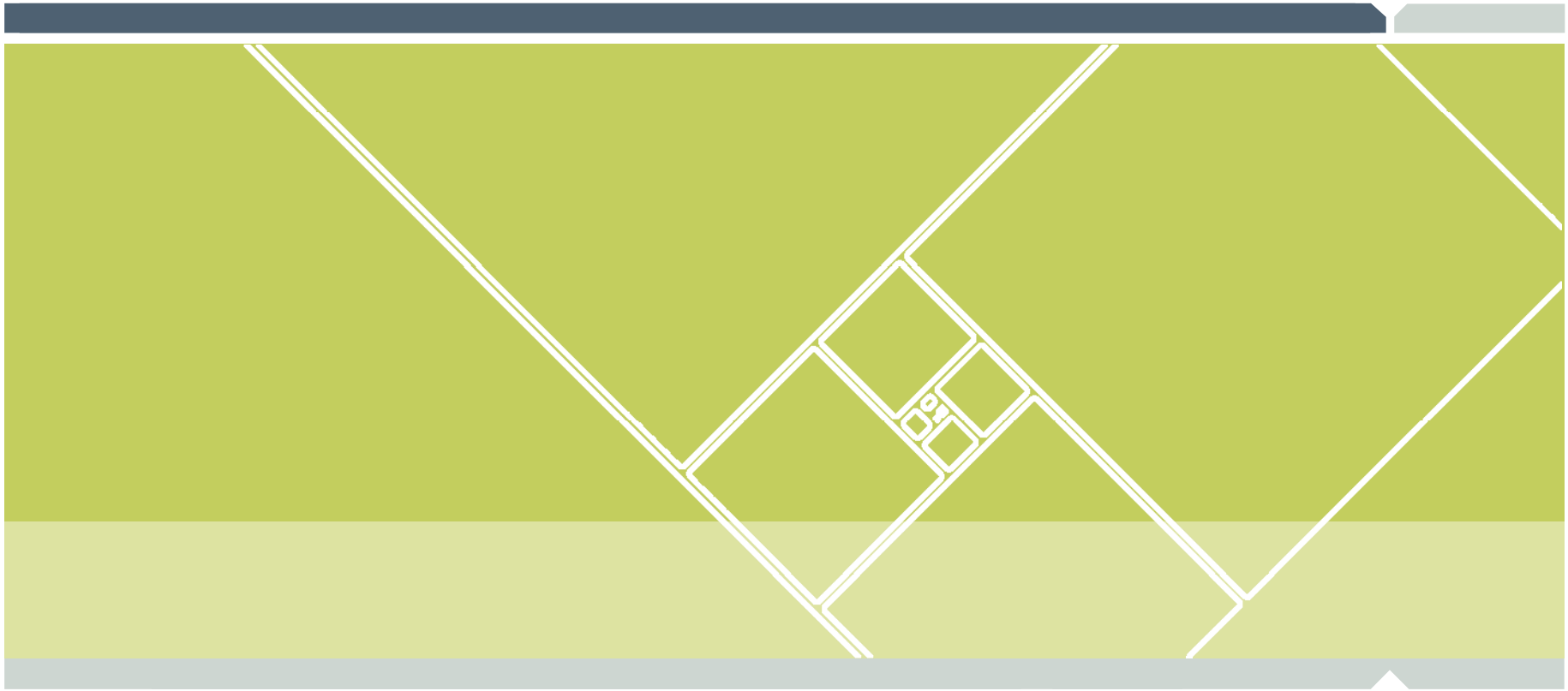

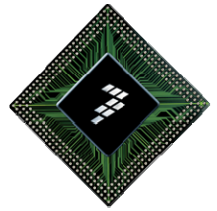

3. Power Mode Control

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Power Control Overview

- ***Mode Entry Control***
- ***Power Control Unit and Reset Generation Module***
- ***Wakeup Unit***
- ***Voltage Regulator and Power Supply***

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Mode Entry Control

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Mode Entry Purpose

- The purpose of the Mode Entry (ME) is to centralize the control of all device modes and related modules / parameters within a unique module

- The ME simplify the implementation of mode management and so increase its robustness
  - Avoiding to manage the power modes on a module by module basis (e.g. peripherals, FLASH mode, voltage regulator)
  - Defining the available modes and their related configuration
  - Providing a SAFE mode to manage HW failure

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Mode Overview

- Provide SYSTEM modes and USER modes
  - SYSTEM: RESET, DRUN (Default RUN), SAFE and TEST
  - USER: RUN(0..3), HALT, STOP and STANDBY
- For each mode the following parameters are configured/controlled
  - System clock sources (ON/OFF)
  - System clock source selection
  - Memory (flash and RAM) power mode (ON, low power, power down)
  - Pad output driver state
  - Peripherals' clock (gated/clocked)
  - Power domains
- Control without CPU intervention the target mode's parameters and mode transition

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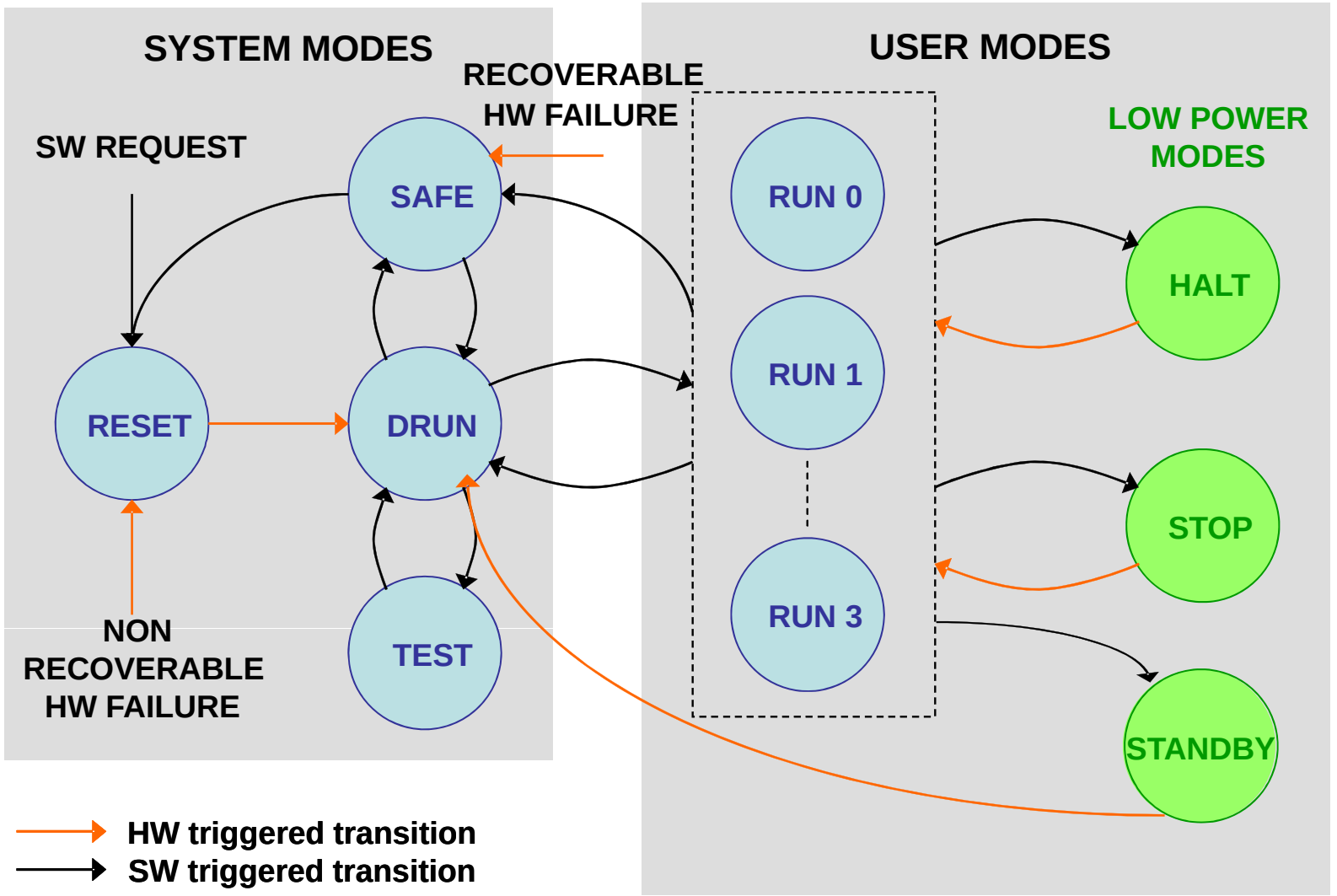
Mode Flow Chart



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System Modes Description

- RESET
  - Virtual mode completely managed by HW
  - The flash initialization is executed while device in RESET
- DRUN (Default RUN)
  - Mode automatically entered out of RESET or STANDBY
  - This mode is used by the application to configure the device out of RESET or out of STANDBY
- SAFE
  - Mode automatically entered on “recoverable HW failure detection” like oscillator, PLL or voltage failure
  - Device in a SAFE configuration with IRC, output high impedance (if configured so)
- TEST
  - Allow device self tests like flash checksum, RAM BIST

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User Modes Description

- RUN[0..3]
  - Full performance available
  - Support WAIT instruction to stop the core with the capability to restart with very short latency (< 4 system clocks)
- HALT
  - Core stopped but system clock can remain the same as in RUN mode
  - Selective peripheral clock gating
  - Flash can be put in low power mode
  - Useful to reduce device consumption during a slow serial communication e.g. LIN frame transmission or reception
- STOP
  - Core stopped, limited clock sources e.g. no PLL available
  - Selective peripheral clock gating
- STANDBY
  - Mode providing the lowest possible consumption
  - Most functions (digital and analog) of the device are not powered
  - Remains only the back-up logic (e.g. RTC/API, Wake-up lines, RAM)

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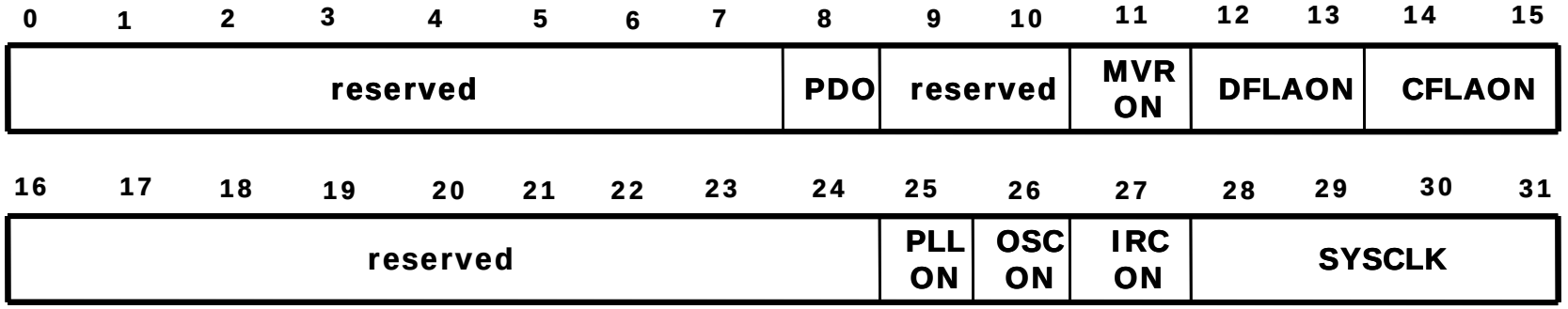
Mode Configuration Register

- Each mode has a Mode Configuration register ME_XXX_MC, where XXX is the mode, e.g. RUN0, HALT, STOP etc.



- PDO: control pad driver output
- MVRON: control VREG on/off
- CFLAON/DFLAON:
  control code / data flash module
  - Normal
  - Low Power
  - Power Down
- PLLON: control PLL on/off
- OSCON: control XOSC on/off
- IRCON: control IRC16M on/off
- SYSCLK: select system clock

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Configuration Parameter

		PDO	MVR	DATA FLASH	CODE FLASH	PLL	OSC	IRC
RESET	RESET	OFF	ON	NORMAL	NORMAL	OFF	OFF	ON
TEST	USER	√	ON	√	√	√	√	√
	RESET	OFF		NORMAL	NORMAL	OFF	OFF	ON
SAFE	USER	√	ON	NORMAL	NORMAL	OFF	OFF	ON
	RESET	ON						
DRUN	USER	OFF	ON	√	√	√		ON
	RESET			NORMAL	NORMAL	OFF	OFF	
RUNx	USER	OFF	ON	√	√	√	√	ON
	RESET			NORMAL	NORMAL	OFF	OFF	
HALT	USER	OFF	√	√	√	√	√	√
	RESET		ON	LOW POWER	LOW POWER	OFF	OFF	ON
STOP	USER	√	√	√	√	OFF	√	√
	RESET	OFF	ON	POWER DOWN	POWER DOWN		OFF	ON
STBY	USER	ON	OFF	POWER DOWN	POWER DOWN	OFF	OFF	√
	RESET							ON

√ CONFIGURABLE

NOT CONFIGURABLE

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System Clock Configuration

MODE / SYSTEM	RESET	TEST	SAFE	DRUN	HALT	STOP	STBY
IRC	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	
IRC_DIV		√		√	√	√	
XOSC		√		√	√	√	
XOSC_DIV		√		√	√	√	
PLL		√		√	√		
NO CLK		√				√	DEFAULT

√ CONFIGURABLE

NOT CONFIGURABLE

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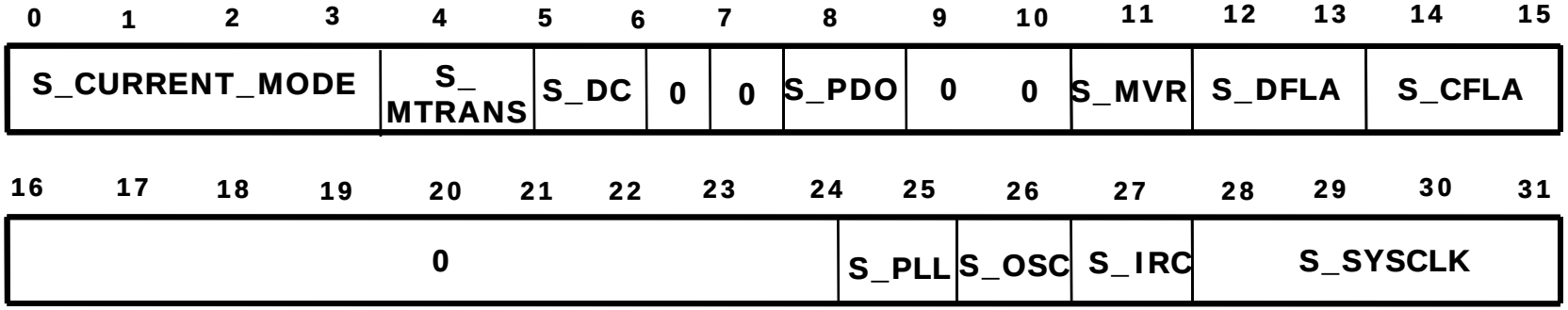
Global Status Register

- Global Status register ME_GS gives the status of the current mode / configuration



- S_MTRANS: transition status
- S_DC: current consumption
- S_PDO: control pad status
- S_MVR: VREG status
- S_DFLA: data flash status
- S_CFLA: code flash status
- S_PLL: PLL status
- S_OSC: XOSC status
- S_IRC: IRC16M status
- S_SYSCLK: system clock status

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SW and HW Transition

- Software handled transition
  - A transition is requested writing a key protected sequence in ME_MCTL
  - Mode Entry configures the modules according to the ME_xxx_MC register of the target mode
  - Once all modules are ready the new mode is entered
  - Transition completion signaling: status bit/interrupt
  - Note: Modification of a ME_xxx_MC register (even the current one) is taken into account on next mode “xxx” entry

- Hardware triggered transition
  - Exit from low power mode
  - SAFE transition caused by HW failure

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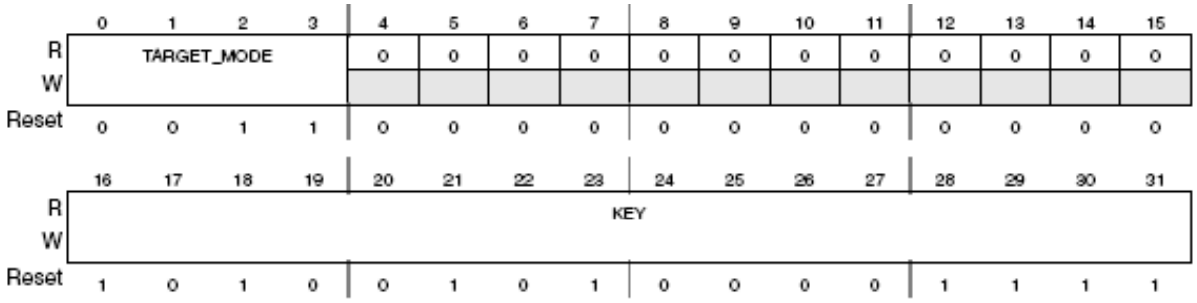
Mode Control Register

- Mode transition is controlled by writing twice ME_MCTL register
  - 1st write: TARGET_MODE + KEY
  - 2nd write: TARGET_MODE + INVERTED KEY

TARGET_ MODE	0000 RESET 0001 TEST 0010 SAFE 0011 DRUN 0100 RUN0 0101 RUN1 0110 RUN2 0111 RUN3 1000 HALT0 1010 STOP0 1101 STANDBY0 others configuration are reserved
KEY	KEY: 0x5AF0 INVERTED KEY: 0xA50F



ME_MCTL register

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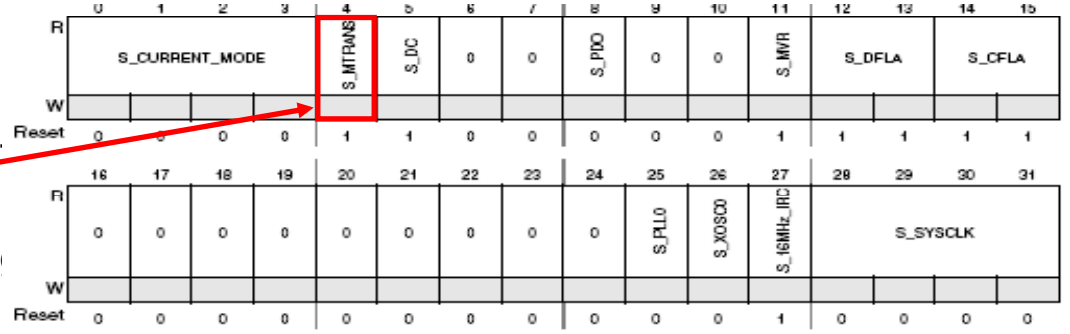
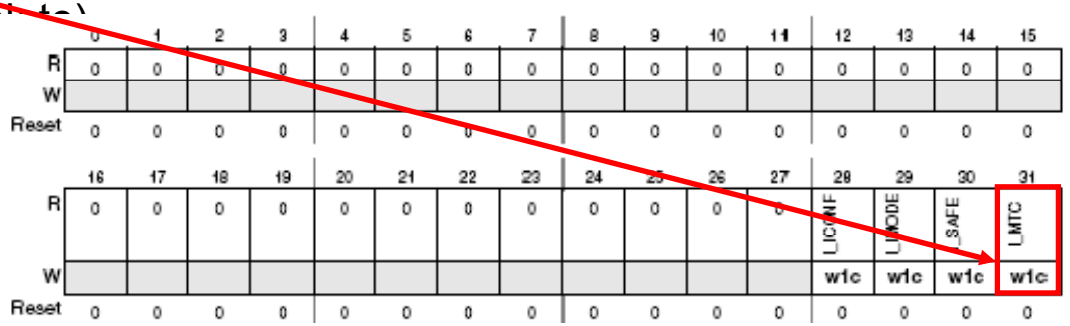
Status and Interrupt

- The complete transition could be triggered by
  - S_MTRANS bit of Global Statu Register (ME_GS)
    - S_MTRANS = 0 (Transition no active)
    - S_MTRANS = 1 (Transition on
  - I_MTC bit of Interrupt Status Register (ME_IS)
    - I_MTC = 0 (No transition comp
    - I_MTC = 1 (Transition complet
- Note: bit I_MTC is not set in case of transition to low pov modes (HALT / STOP / STANDBY0)



ME_GS register



ME_IS register

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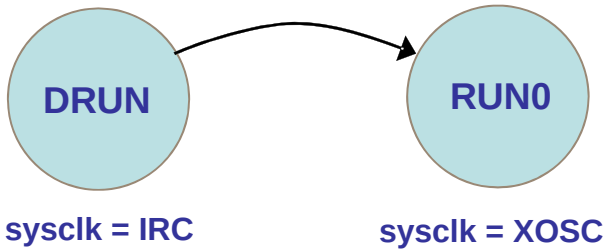
Example 1 of 3 DRUN Mode → RUN0 Mode transition

- Current Mode: DRUN with system clock = IRC (default)
- Target Mode: RUN0 Mode with system clock = XOSC

Steps

- Configuration of RUN0 Mode
  - ME_RUN0_MC.OSCON = 1
  - ME_RUN0_MC.SYSCLK = XOSC
- Transition request
  - ME_MCTL = RUN0 + KEY
  - ME_MCTL = RUN0 + INVERTED KEY
- Waiting for the transition complete through the ME_IS.I_MTC bit



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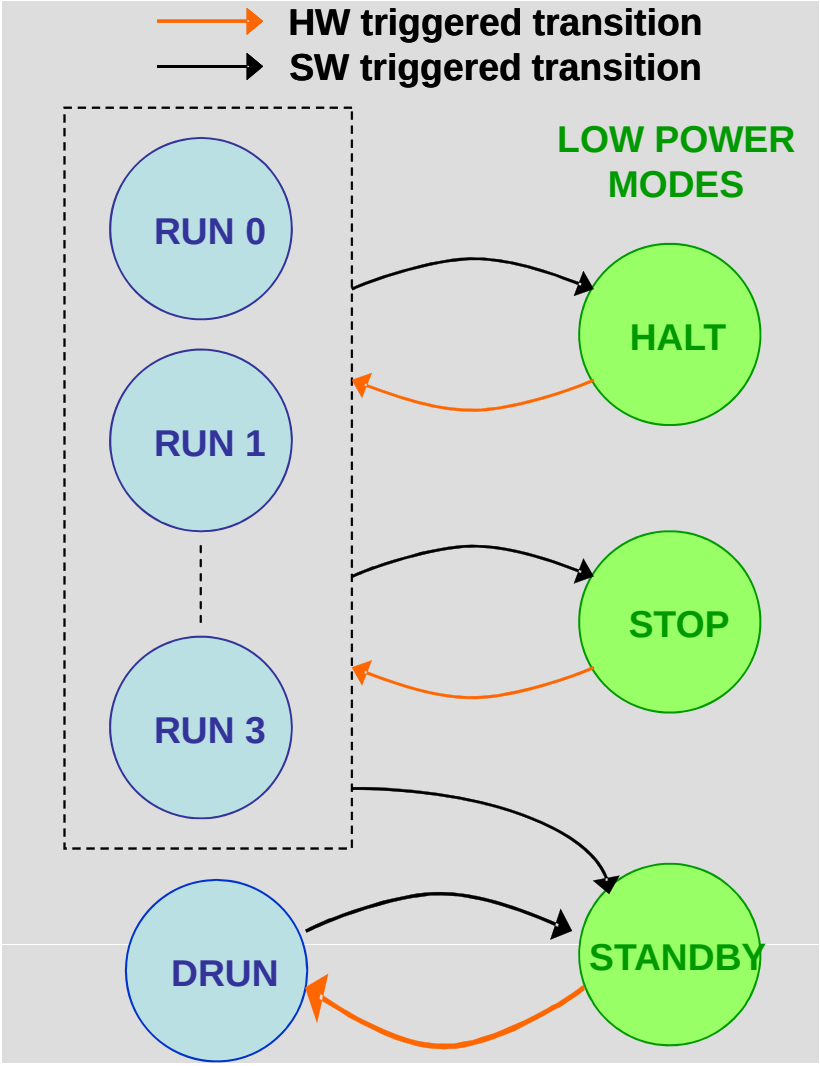
Exit Low Power Mode

- Automatically managed by hardware
- Came back to the previous mode from which entered in if exit from Stop mode



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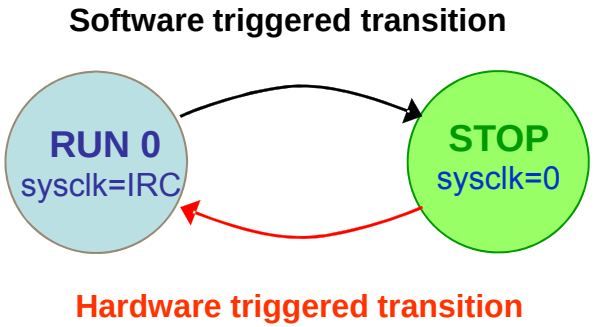
Example 2 of 3 RUN0 Mode → STOP Mode → RUN0 Mode transition

- Configuration of STOP Mode
  - ME_STOP_MC.SYSCLK = NO CLK
- Software Transition request
  - ME_MCTL = STOP + KEY
  - ME_MCTL = STOP + INVERTED KEY
  - Device put in STOP Mode by SW
- Force an interrupt / wakeup event
- Device exited from STOP Mode to RUN0 Mode by HW
- Waiting for the transition complete through the ME_IS.I_MTC bit



RUN 0 with system clock = IRC (default)
STOP mode with no system clock

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Interrupt Management

- The mode entry can generate interrupts on the following events
  - Invalid mode event
    - Mode configuration
    - Mode transition
  - SAFE Mode transition event on HW request
  - Mode transition event complete
- Each interrupt flag can be masked independently

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Invalid Mode Configuration

- Caused by writing ME_<mode>_MC registers with invalid mode configuration
- I_ICONF bit in the Interrupt Status register ME_IS
- To avoid invalid mode configuration event
  - IRC should be ON if: sysclk = rc_clk or sysclk = rc_clk_div
  - XOSC should be ON if: sysclk = osc_clk or sysclk = osc_clk_div
  - PLL should be ON if: sysclk = pll_clk
  - Configuration “00” for the CFLAON and DFLAON bit fields should not be used
  - MVR must be ON if any of the following is active: PLL/CFLASH/DFLASH
  - System clock configurations marked as ’reserved’ may not be selected
  - Configuration “1111” for the SYSCLK bit field is allowed only for STOP0 and TEST modes

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	I_ICONF	I_IMODE	I_SAFE	I_MTC
W													w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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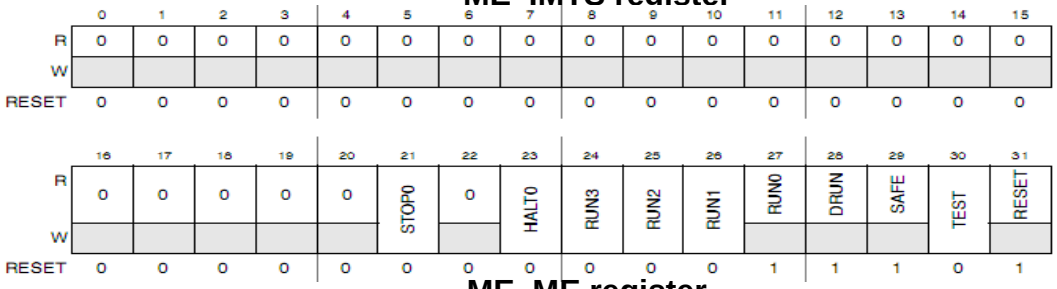
Invalid Mode Transition

- I_ICONF bit in the Interrupt Status register
- Five causes revealed by Inva
- Mode Transition Status regist
  - Mode Transition Illegal
    - Mode requested when a transition is active
  - Mode Request Illegal
    - Target mode not valid respect to current
  - Disable Mode Access
    - Target mode is disabled in Mode Enable Register
  - Non Existing Mode Access
    - Target mode doesn't exist
  - SAFE Event Active Status
    - Transition is requested when bit is pending

ME_IS register

ME_IMTS register



ME_ME register

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Peripheral Clock Gating

- The Mode Entry Module manages the clock gating of each peripheral
- Define peripherals' state (active/frozen) in each mode
  - 8 different types of peripheral behavior during running modes
  - 8 different types of peripheral behavior during low power modes

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RUN/LP Configuration Registers

- ME_RUN_PC[0…7] registers configure the behavior of peripherals during RUN Modes
- ME_LP_PC[0…7] registers configure the behavior of peripherals during Low Power Modes
- Configuration bits
  - 0: peripheral is frozen with clock gated
  - 1: peripheral is active

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	RUN3	RUN2	RUN1	RUN0	DRUN	SAFE	TEST	RESET
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Run Peripheral Configuration Registers (ME_RUN_PC0...7)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	STOP0	0	HALT0	0	0	0	0	0	0	0	0
W																
RESET	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Low-Power Peripheral Configuration Registers (ME_LP_PC0...7)

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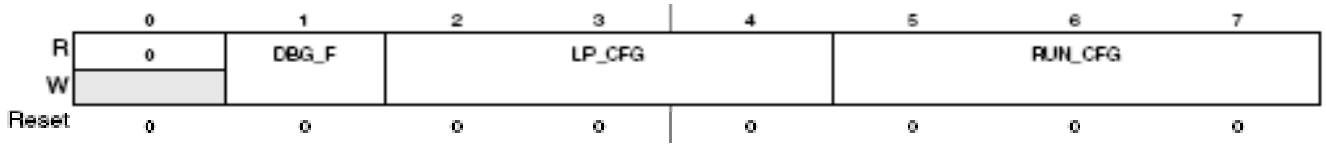
Peripheral Control Registers

- ME_PCTL[0…143] registers select the Running/Low Power Mode configurations for each peripheral



Peripheral Control Registers (ME_PCTL0…143)

- DBG_F bit controls the state of the peripheral in Debug Mode
  - 0: peripheral status depends on LP_CFG / RUN_CFG
  - 1: peripheral is frozen
- LP_CFG bits specify a Low Power Mode configuration as defined in ME_LP_PCs
  - 000: select the ME_LP_PC[0] configuration
  - …
  - 111: select the ME_LP_PC[7] configuration
- RUN_CFG bits specify a Running Mode configuration as defined in ME_RUN_PCs
  - 000: select the ME_RUN_PC[0] configuration
  - …
  - 111: select the ME_RUN_PC[7] configuration

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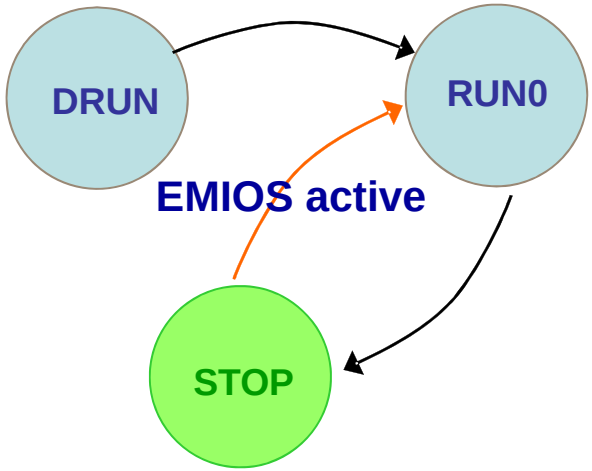
Example 3 of 3 EMIOS0 Clock Gating

- Configure EMIOS in the following way
  - Active in DRUN,RUN0,STOP Mode
  - Clock gated in the others mode
- Steps
- Configuration of Running Mode
  - ME_RUN_PC[1].DRUN = 1
  - ME_RUN_PC[1].RUN0 = 1
- Configuration of Low Power Mode
  - ME_LP_PC[2].STOP = 1
- Configuration of EMIOS (peripheral number = 72)
  - ME_PCTL[72].RUN_CFG = 1
  - ME_PCTL[72].LP_CFG = 2



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Power Control Unit

and Reset Generation Module

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Power Control unit

- The MCU peripherals are allocated to various power domains
- The PCU allows users to remove or apply power to a power domain depending on the operating mode
  - This is used to optimise power saving
- Each time the MCU changes mode, the PCU:
  - Evaluates the required status of each power domain
  - Provides controlled power-up or power-down of the power domain (if required)
- Only one power domain (2) can be controlled by the PCU
  - Power domains 0 & 1 are not controllable
- A status register indicates the current state of each power domain

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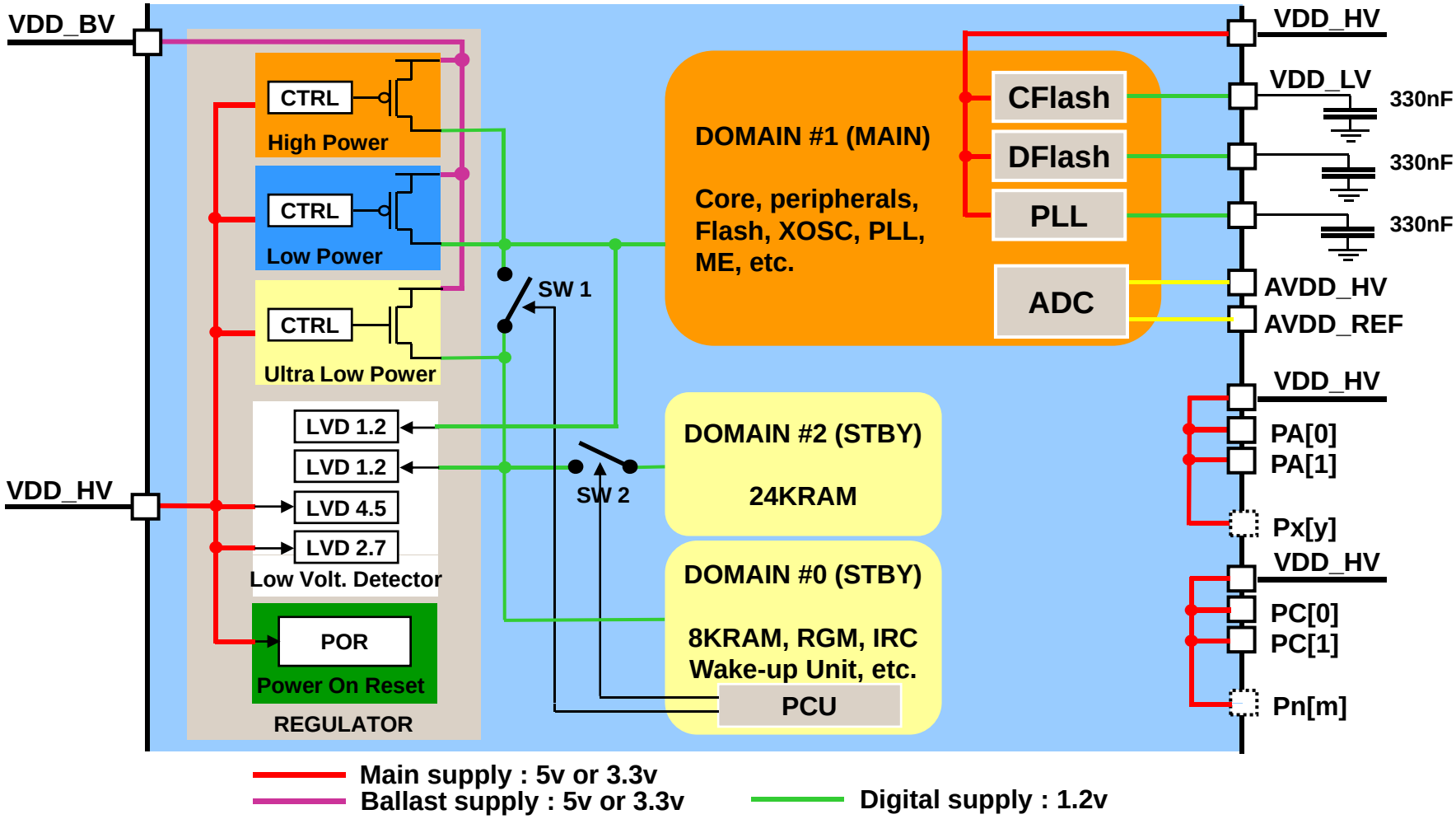
VREG Supply and Regulator Diagram



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Operating modes supported

- The PCU has individual control bits for the following operating modes in the appropriate Configuration Register
  - RESET, DRUN, SAFE, TEST, RUN0, RUN1, RUN2, RUN3, HALT0, STOP0, and STANDBY0
- These bits are available for all power domains but only domain 2 is configurable
  - To enable a power domain set the bit corresponding to each mode
  - By default the power domain is enabled in all modes except STANDBY0 mode

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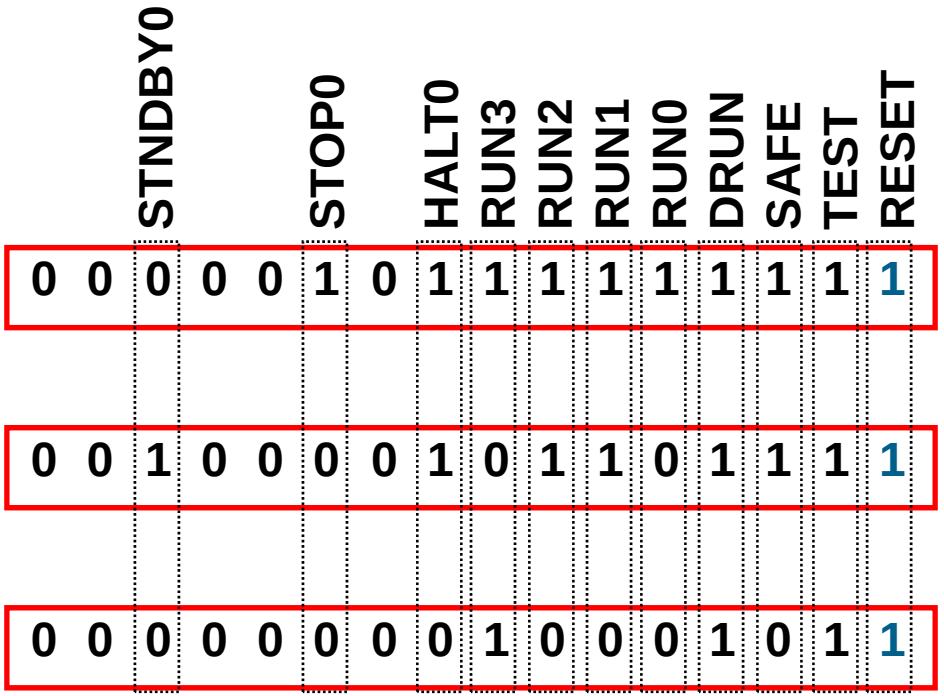
Power Domain 2 Examples



PD2 powered in

All modes *except* STNDBY0

All modes *except* STOP0, RUN3 & RUN0

***Only* RUN3, DRUN & TEST**

RESET bit read-only

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Reset Generation Module

- There are two classes of reset handled by the RGM
  - Destructive resets completely restart the MCU after a critical event
    - Register and memory contents are not guaranteed
  - Functional resets restart digital modules but preserve analog, flash and debugging module settings
- The RGM contains various registers that reflect the status of the MCU and allow users to configure certain reset behaviours
- There are four phases of reset that the RGM provides to ensure correct behaviour
- The RGM handles selection of the boot mode
- Resets can optionally drive the reset pin on an event

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Reset functionality

- Destructive resets
  - Power-on reset
  - 1.2V low-voltage detected (power domain #0 or #1)
  - 2.7V low-voltage detected
  - Software watchdog timer*
- Functional resets
  - External reset
  - JTAG initiated reset*†
  - Core reset*†
  - Software reset†
  - Checkstop reset†
  - PLL0 fail*†
  - Oscillator frequency lower than reference*†
  - CMU0 clock frequency higher/lower than reference*†
  - 4.5V low-voltage detected*†
  - Code or data flash fatal error*†

* Can optionally create an interrupt request or a safe mode request
† Can optionally choose a short reset sequence

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Notes

- When power is removed from a domain all of the status and contents of memories and registers is lost
- Typically RAM is split across two domains with a small block preserved even in STANDBY0 mode
- The primary domain (0) is always powered even in STANDBY0 mode as wakeup unit is located in this domain.

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Voltage Regulator and Power Supply

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VREG Supply Pin

- VDD_HV/VSS_HV (4x pairs) Digital Supply Voltage
  - Range: 5V or 3.3V
  - Supply modules: I/O, clock sources, flash HV part
- VDD_BV (1x pair) Ballast Voltage
  - Range: 5V or 3.3V
  - Supply the ballast transistors of all internal voltage regulators
- VDD_LV (3x pairs) Internal Digital Low Voltage
  - Internal 1.2V decoupling pins
  - 330nF capacitor must be placed between VDD_LV and VSS_LV
- VDD_HV_ADC/VSS_HV_ADC (1x pair)
  - Range: 5V or 3.3V
  - Supply ADC module only

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VREG Regulator Main Features

- 3 Regulators
  - High power or main regulator
  - Low power regulator
  - Ultra low power regulator
- 4 Low Voltage Detectors
  - Low voltage detector for 5.0v on the main supply
  - Low voltage detector for 3.3v on the main supply
  - Low voltage detector for 1.2v on main digital domain
  - Low voltage detector for 1.2v on standby domain
- Power On Reset

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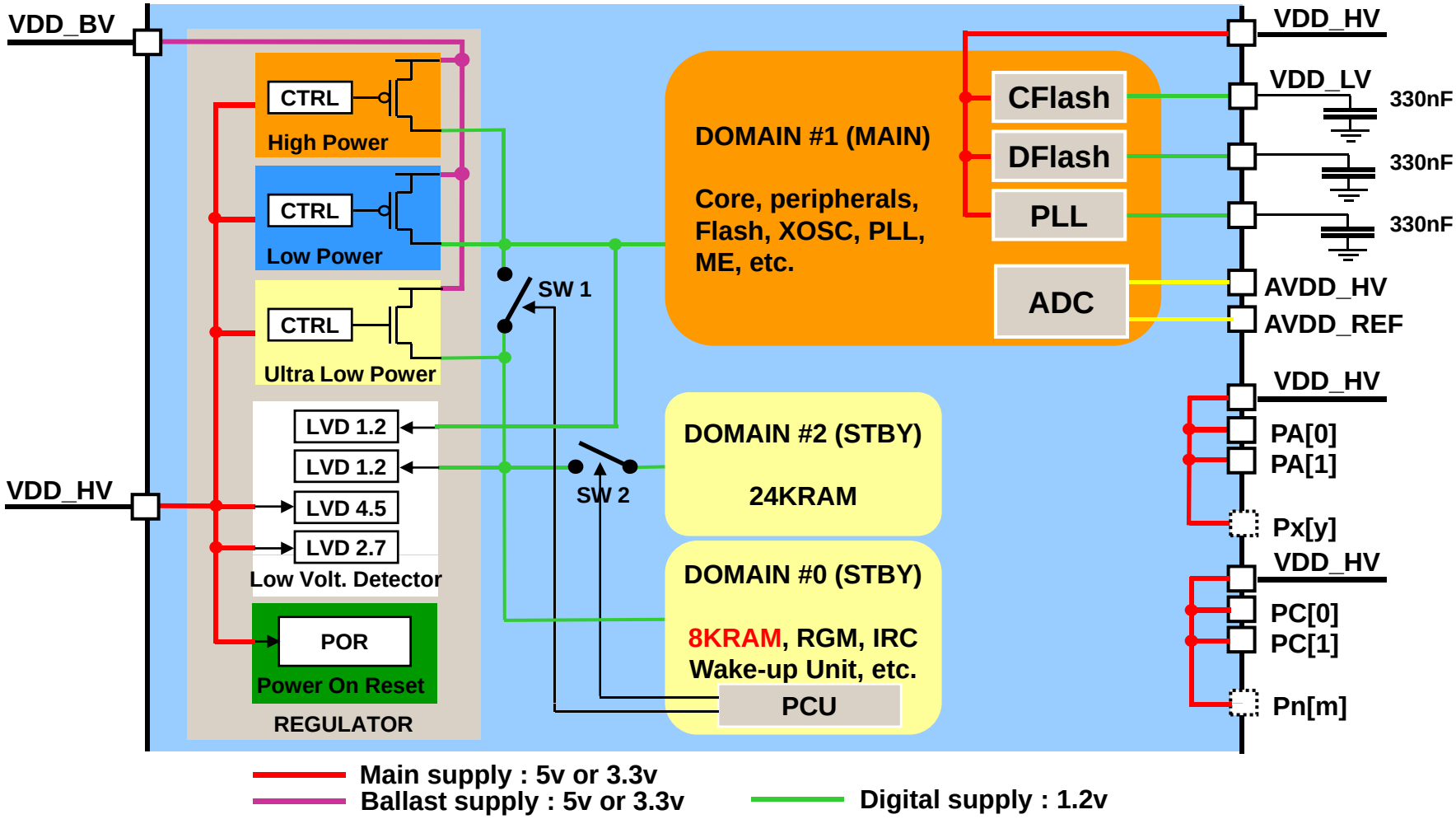
VREG Supply and Regulator Diagram



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VREG Regulator Different Mode- Main Functions Summary

VREG Regulator	Power Domain	Input Voltage	Output Supply	Externally Cap	Control and regulation integrated into the chip
High Power Regulator	1.2v digital power	3.3v to 5.0v +/- 10%	1.2v +/- 10% / up to **100**mA	minimum of 3 x 330nF cap	PMOS
Low Power	1.2v digital power in STOP mode	3.3v to 5.0v +/- 10%	1.2v +/- 10% / up to **15**mA	minimum of 3 x 330nF cap	PMOS
Ultral Low Power Regulator	1.2v digital power in STANDBY mode	3.3v to 5.0v +/- 10%	1.2v +/- 10% / up to **5**mA	No externally capacitance needed	NMOS

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VREG Low Voltage Detectors - Main functions

- Low voltage detector for 5.0v operations on the main supply
  - Upper level : 4.37v max.
  - Lower level : 4.2v min.
- Low voltage detector for 3.3v operations on the main supply
  - Upper level : 2.8v typ.
  - Lower level : 2.7v typ.
- Low voltage detector for 1.2v on the digital core supplies
  - Monitor 1.2v on main & low power regulator (in run or stop mode)
  - Monitor 1.2v on ultra low power regulator (in standby mode)
  - Upper level : 1.185v max.
  - Lower level : 1.095v min.

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VREG Power On Reset - Main functions

- Works only on the rising edge of the main supply
- Used to mask all 1.2v controls signals during supply ramp
- POR levels : 1.5v to 2.7v

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Wakeup Unit

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Wakeup Unit

The Wakeup Unit supports 2 internal sources (WKUP[0:1]) and up to 18 external sources (WKUP[2:19]) that can generate interrupts or wakeup events, of which WKUP2 can cause non-maskable interrupt requests.

The Wakeup Unit supports these distinctive features:

- Non-maskable interrupt support with
  - 1 NMI source with bypassable glitch filter
  - Independent interrupt destination: non-maskable interrupt, critical interrupt, or machine check request
  - Edge detection
- External wakeup/interrupt support with
  - 3 system interrupt vectors for up to 18 interrupt sources
  - Analog glitch filter per each wakeup line
  - Independent interrupt mask
  - Edge detection
  - Configurable system wakeup triggering from all interrupt sources
  - Configurable pullup
- On-chip wakeup support
  - 2 wakeup sources
  - Wakeup status mapped to same register as external wakeup/interrupt status

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Wakeup Line Mapping

Wakeup Number	MPC560xB		
	Port	SIU_PCR #	Wakeup IRQ to INTC
WKUP0	API	n.a.	WakeUp_IRQ_0
WKUP1	RTC	n.a.	WakeUp_IRQ_0
WKUP2	PA1	PCR1	WakeUp_IRQ_0
WKUP3	PA2	PCR2	WakeUp_IRQ_0
WKUP4	PB1	PCR17	WakeUp_IRQ_0
WKUP5	PC11	PCR43	WakeUp_IRQ_0
WKUP6	PE0	PCR64	WakeUp_IRQ_0
WKUP7	PE9	PCR73	WakeUp_IRQ_0
WKUP8	PB10	PCR26	WakeUp_IRQ_1
WKUP9	PA4	PCR4	WakeUp_IRQ_1
WKUP10	PA15	PCR15	WakeUp_IRQ_1
WKUP11	PB3	PCR19	WakeUp_IRQ_1
WKUP12	PC7	PCR39	WakeUp_IRQ_1
WKUP13	PC9	PCR41	WakeUp_IRQ_1
WKUP14	PE11	PCR75	WakeUp_IRQ_1
WKUP15	PF11	PCR91	WakeUp_IRQ_1
WKUP16	PF13	PCR93	WakeUp_IRQ_2
WKUP17	PG3	PCR99	WakeUp_IRQ_2
WKUP18	PG5	PCR101	WakeUp_IRQ_2
WKUP19	PA0	PCR0	WakeUp_IRQ_2

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External Wakeups/Interrupts

The Wakeup Unit supports up to 18 external wakeup/interrupts which can be allocated to any pad necessary at the SoC level. This allocation is fixed per SoC.

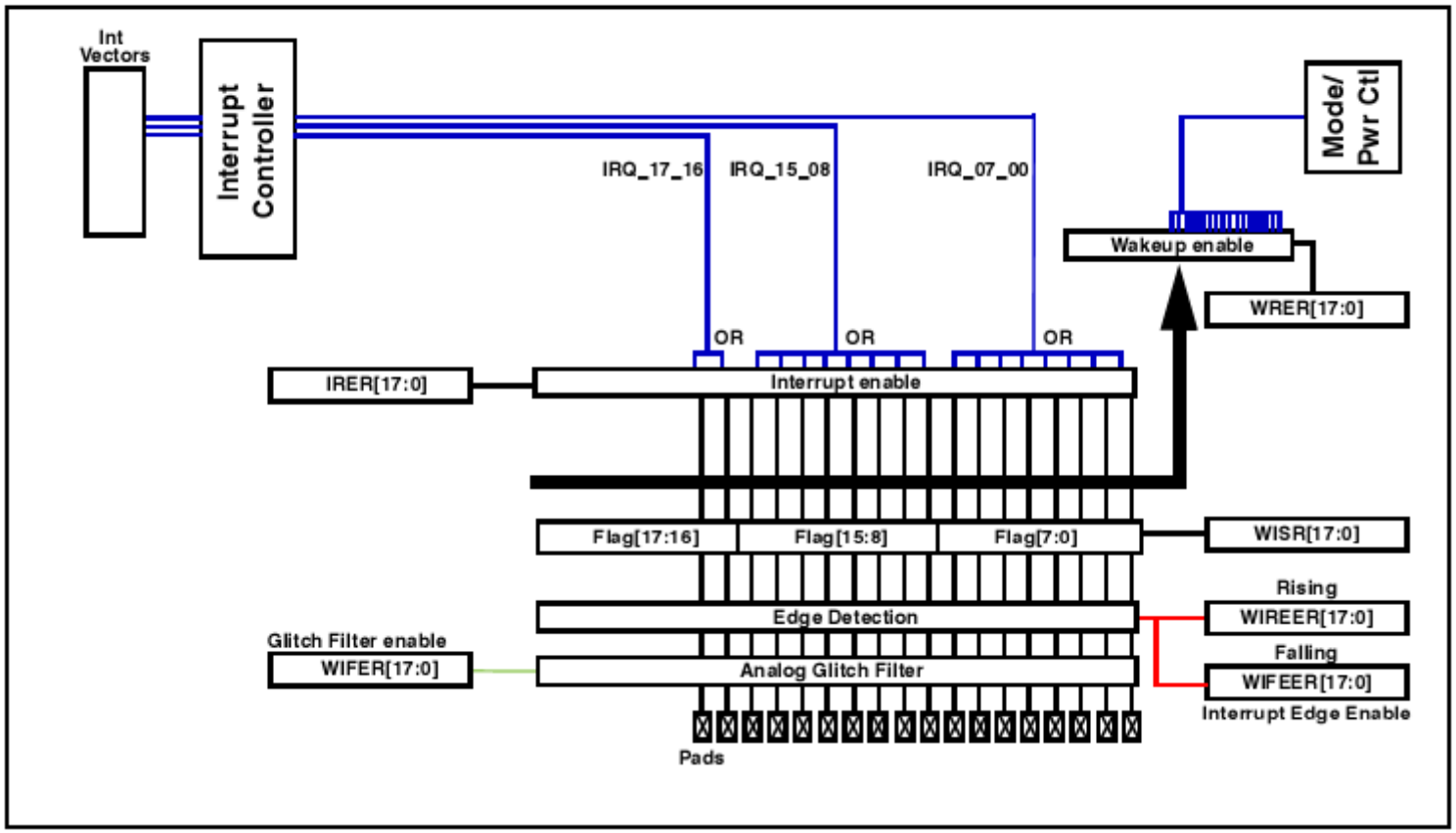

Figure 28-4. External Interrupt Pad Diagram

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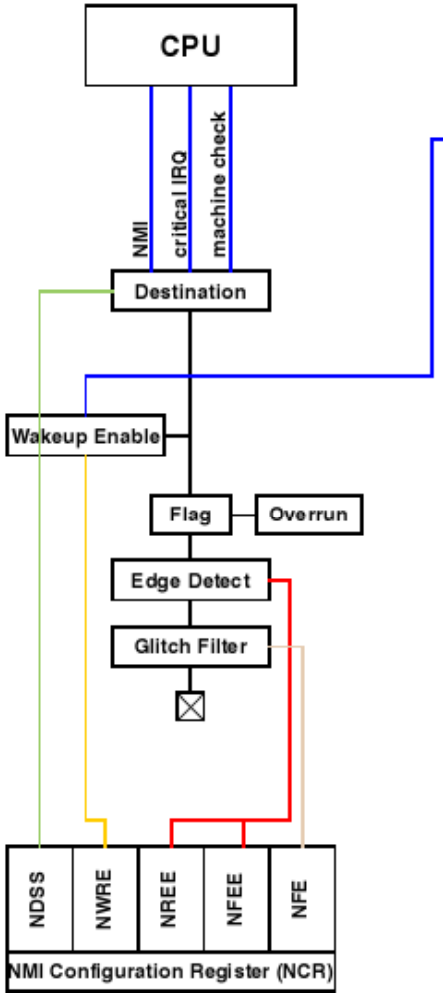
Non-Maskable Interrupts

External pin — PA[1], GPIO[1], E0UC[1], NMI[0], WKUP[2]



NMI pad diagram

The Wakeup Unit supports the generation of three types of interrupts from the NMI. The Wakeup Unit supports the capturing of a second event per NMI input before the interrupt is cleared, thus reducing the chance of losing an NMI event.

Each NMI passes through a bypassable analog glitch filter.

NMI Configuration Register (NCR)

NDSS[x]	NMI Destination Source Select x. 00 Non-maskable interrupt 01 Critical interrupt 10 Machine check request 11 Reserved - no NMI, critical interrupt, or machine check request generated
NWRE[x]	NMI Wakeup Request Enable x. 1 A set NIF[x] bit or set NOVF[x] bit causes a system wakeup request 0 System wakeup requests from the corresponding NIF[x] bit are disabled
NREE[x]	NMI Rising-edge Events Enable x. 1 Rising-edge event is enabled 0 Rising-edge event is disabled
NFEE[x]	NMI Falling-edge Events Enable x. 1 Falling-edge event is enabled 0 Falling-edge event is disabled
NFE[x]	NMI Filter Enable x. Enable analog glitch filter on the NMI pad input. 1 Filter is enabled 0 Filter is disabled

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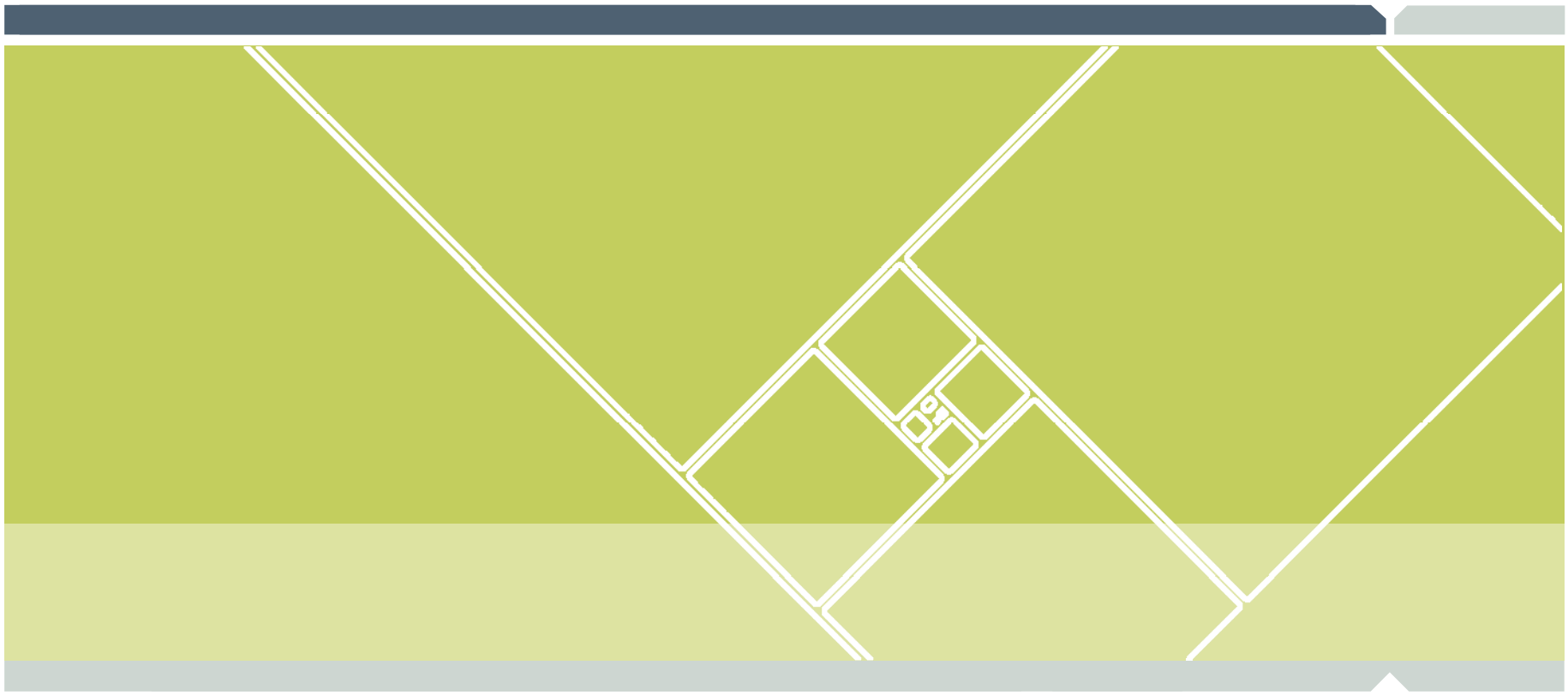

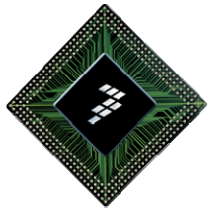

5. Memory

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Memory Topics

- ***Memory Map***
- ***Flash Memory***
    - **** Code Flash***
    - **** Data Flash***
- ***SRAM***
- ***MPU***
- ***ECC***

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Memory Map

Table 1-4 shows the memory map for the MPC5604B. All addresses on the MPC5604B, including those that are reserved, are identified in the table. The addresses represent the physical addresses assigned to each IP block.

Table 1-4. Memory map

Start address	End address	Size (KB)	Region name
0x00000000	0x00007FFF	32	Code Flash Sector 0
0x00008000	0x0000BFFF	16	Code Flash Sector 0
0x0000C000	0x0000FFFF	16	Code Flash Sector 0
0x00010000	0x00017FFF	32	Code Flash Sector 0
0x00018000	0x0001FFFF	32	Code Flash Sector 0
0x00020000	0x0003FFFF	128	Code Flash Sector 0
0x00040000	0x0005FFFF	128	Code Flash Sector 0
0x00060000	0x0007FFFF	128	Code Flash Sector 0

. . .

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Flash Memory

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Flash Memory Architecture

The Flash memory comprises a platform Flash controller (PFlash) interface and two Flash memory arrays: one array of 512 Kbyte for code (CFlash) and one array of 64 Kbyte for data (DFlash). The Flash architecture of this device is illustrated in Figure 19-1.

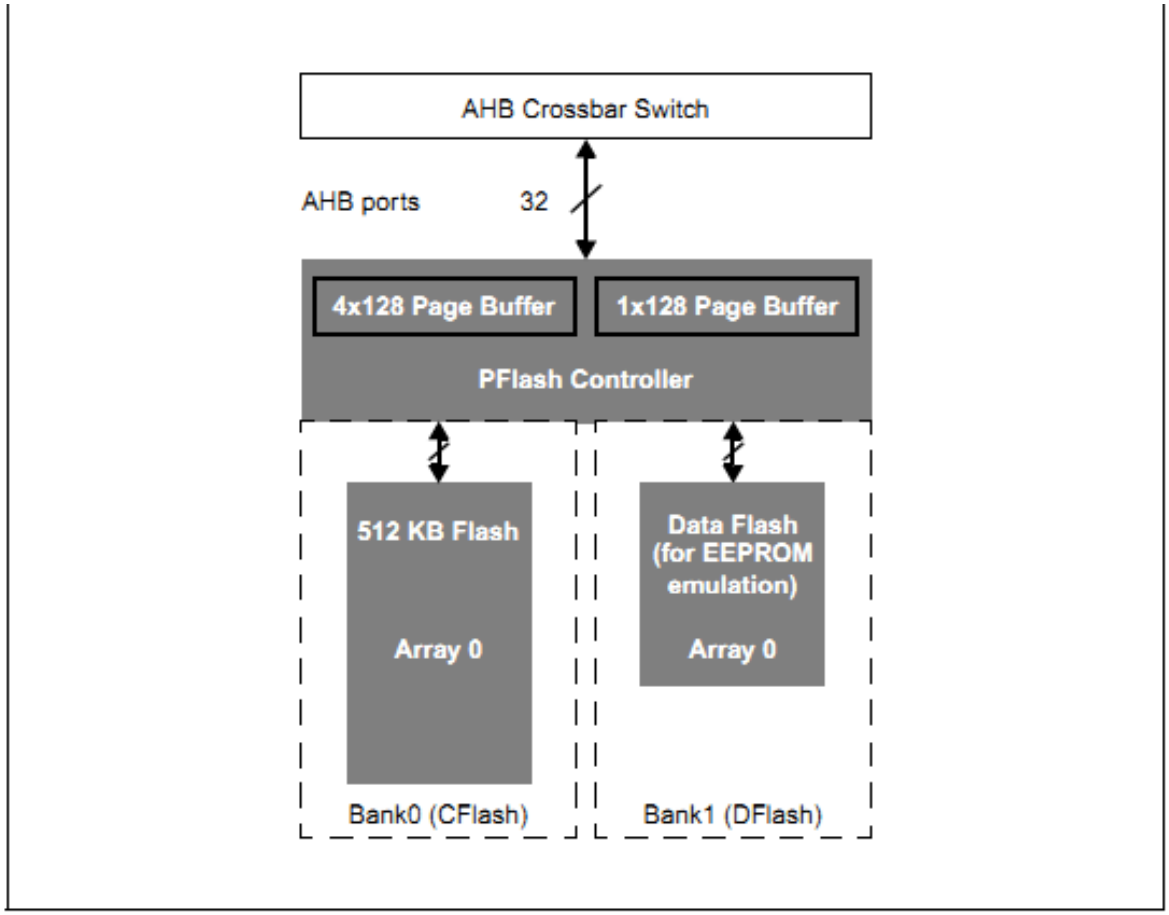

Figure 19-1. Flash memory architecture

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Code Flash Module Structure

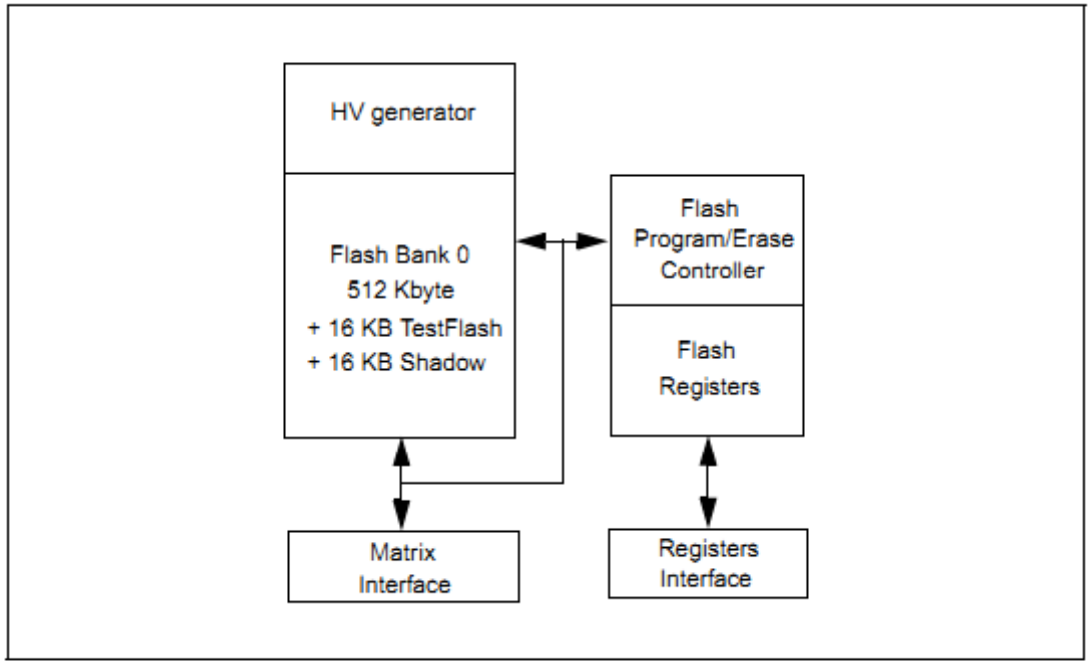

Figure 19-2. Flash module structure

❖ Code Flash composed of single blank with 512K Flash memory: RWW is not supported.

❖ Addressable double words(64bits) for programming, and page (128bits)for reading.

❖ 16 KB TestFlash is exists out side the normal address space and is programmed and read independently of other blocks. The TestFlash is reserved to store the non-volatile information about redundancy, configuration and protection.

❖ The 16 KB shadow section is presented to store user defined functions (possibly to store boot code, other configuration words or factory process codes).

❖ The Flash module supports fault tolerance through Error Correction Code (ECC) or error detection, or both. The **ECC** implemented within the Flash module will correct single bit failures and detect double bit failure.

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Data Flash Module Structure

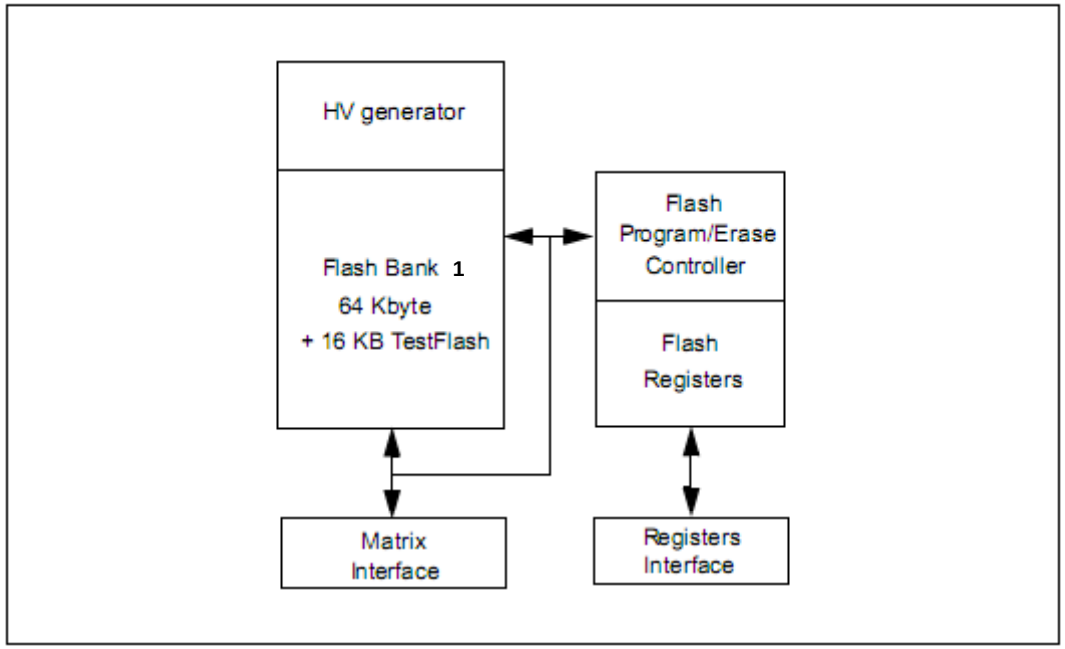

Figure 20-26. Flash module structure

- ❖ High Read parallelism (128 bits)
- ❖ Error Correction Code (SEC-DED) to enhance Data Retention
- ❖ Double Word Program (64 bits)
- ❖ Sector erase
- ❖ Single bank—Read-While-Write (RWW) not available
- ❖ Erase Suspend available (Program Suspend not available)
- ❖ Software programmable program/erase protection to avoid unwanted writings
- ❖ Censored Mode against piracy
- ❖ Not usable as main Code Memory of the device
- ❖ Shadow Sector not available
- ❖ One-Time Programmable (OTP) area in Test Flash block

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Code Flash Sectorization

Bank 0 of the Flash module is divided in 10 sectors including a reserved sector, named TestFlash, in which some One-Time Programmable (OTP) user data are stored, as well as a Shadow Sector in which user erasable configuration values can be stored.

The matrix module sectorization is shown in Table 19-1.

Table 19-1. Flash module sectorization

Bank	Sector	Addresses	Size	Address space
B0	B0F0	0x000000–0x007FFF	32 Kbyte	Low Address Space
B0	B0F1	0x008000–0x00BFFF	16 Kbyte	Low Address Space
B0	B0F2	0x00C000–0x00FFFF	16 Kbyte	Low Address Space
B0	B0F3	0x010000–0x017FFF	32 Kbyte	Low Address Space
B0	B0F4	0x018000–0x01FFFF	32 Kbyte	Low Address Space
B0	B0F5	0x020000–0x03FFFF	128 Kbyte	Low Address Space
B0	B0F6	0x040000–0x05FFFF	128 Kbyte	Mid Address Space
B0	B0F7	0x060000–0x07FFFF	128 Kbyte	Mid Address Space
B0	Reserved	0x080000–0x1FFFFF	1536 Kbyte	High Address Space
B0	B0SH	0x200000–0x203FFF	16 Kbyte	Shadow Address Space
B0	Reserved	0x204000–0x3FFFFF	2032 Kbyte	Shadow Address Space
B0	B0TF	0x400000–0x403FFF	16 Kbyte	Test Address Space
B0	Reserved	0x404000–0x7FFFFF	4080 Kbyte	Test Address Space

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Flash in Different Modes

- **Reset Mode**
  - ✓ Reset is highest priority for Flash module and will terminates all other operations.
  - ✓ Reset will terminates all other operations and forces Flash into the user mode to receive access.
  - ✓ MCR.DONE may be polled to determine if the Flash module has complete the transition out of Reset, and the registers can not be written until MCR.DONE is set.
- **Power down mode (Disabled-mode)**
  - ✓ All DC current can be turned off in power down mode, so the power dissipation is due only to the leakage of circuitry.
  - ✓ Read and write is not supported in this mode.
  - ✓ If the Flash is disabled during erase operation, it could be suspended and resumed when power down mode is exited.
  - ✓ If the Flash is disable during the program operation, the power down mode will not entered until the program operation completed.
- **Low power mode (sleep-mode)**
  - ✓ Most of DC current can be turned off in low power mode.
  - ✓ Read and write is not supported in this mode.
  - ✓ If the Flash is disabled during erase operation, it could be suspended and resumed when power down mode is exited.
  - ✓ If the Flash is disable during the program operation, the power down mode will not entered until the program operation completed.
- **Normal Mode** – The operational mode of Flash module

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Platform Flash Controller (PCF)

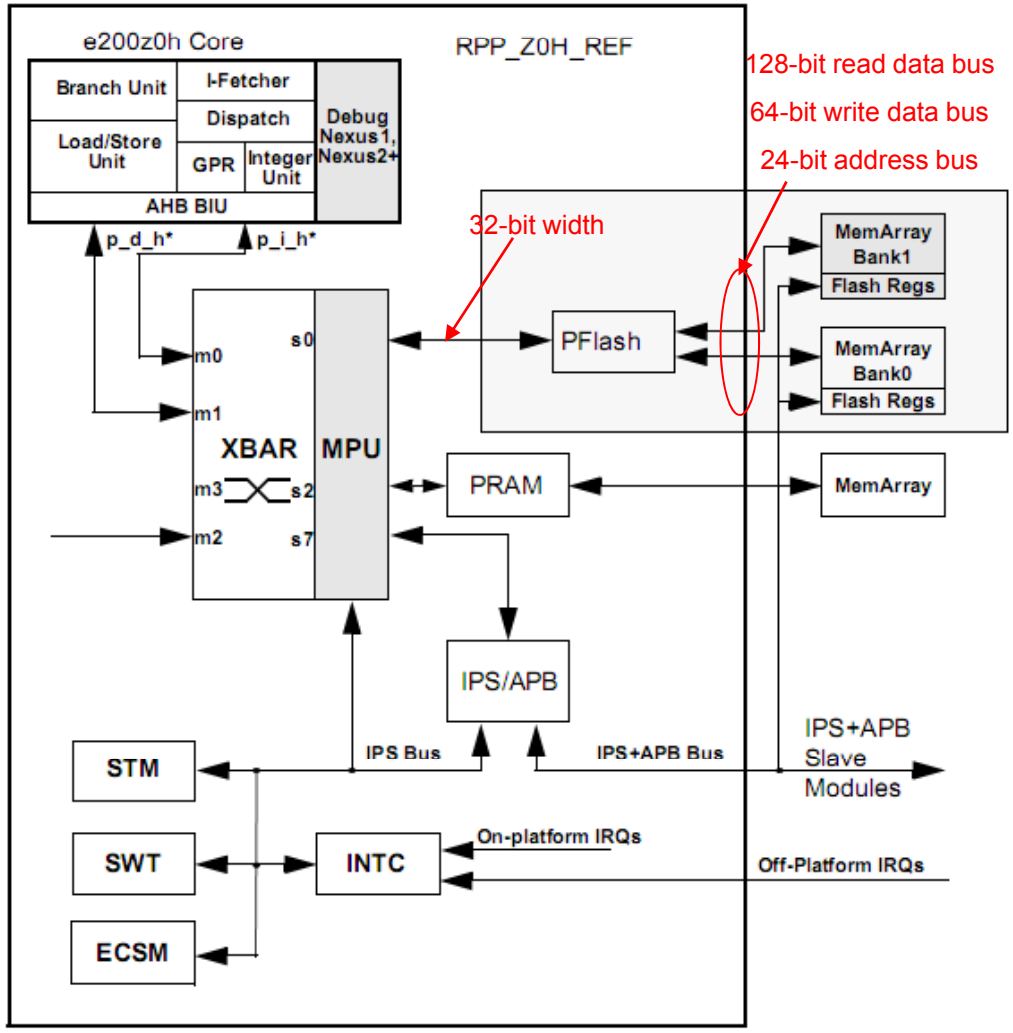

Figure 20-42. Power Architecture e200z0h RPP reference platform block diagram

Key Features of PCF

- ❖ Dual array interfaces support up to a total of 16Mbytes of Flash memory, partitioned as two separate 8 Mbytes backs.
- ❖ Single AHB port interface supports a 32-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported, Only aligned word writes are supported.
- ❖ Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- ❖ Several prefetch control algorithms are available for controlling page read buffer fills.
- ❖ Access protections may be applied on a per-master basis for both reads and writes to support security and privilege mechanisms.

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Flash Prog/Erase Operations

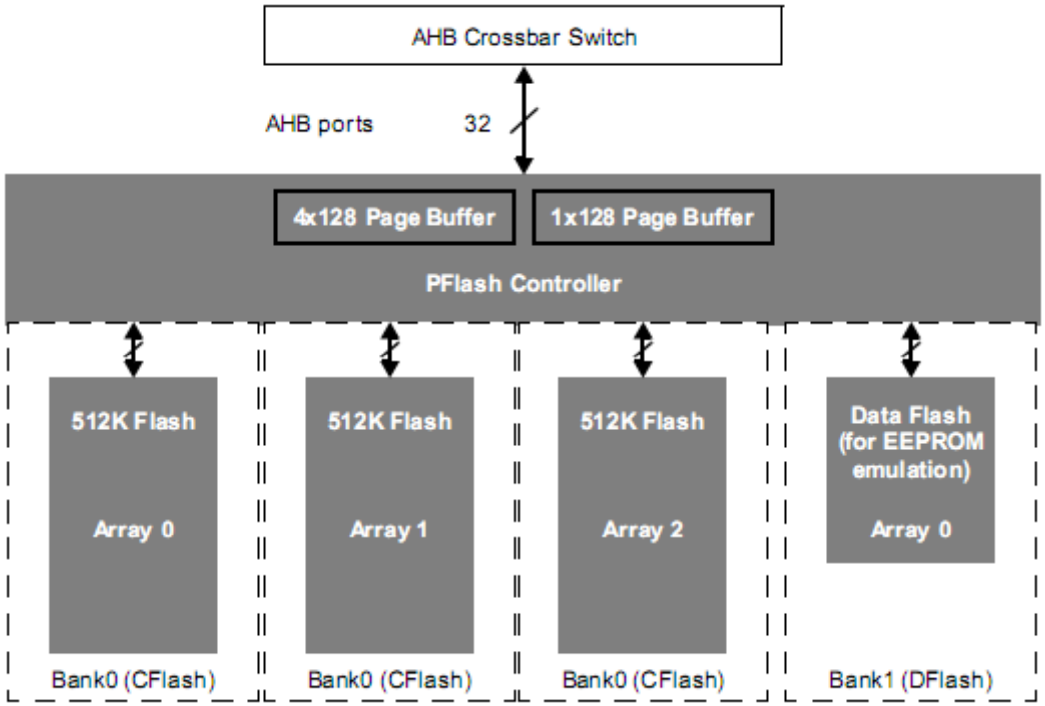

Figure 20-1. Flash memory architecture

Notes

- RWW is not supported in same Bank memory, however supported in different Banks.
- All prog/erase operations of Flash module are managed through the Flash User Registers Interface.

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Flash Prog/Erase Operations (continued)

In general each modify operation is started through a sequence of three steps:

1. The first instruction is used to select the desired operation by setting its corresponding selection bit in MCR (PGM or ERS) or UT0 (MRE or EIE).
2. The second step is the definition of the operands: the Address and the Data for programming or the Sectors for erase or margin read.
3. The third instruction is used to start the modify operation, by setting EHV in MCR or AIE in UT0.

Table 20-62. Flash modify operations

Operation	Select bit	Operands	Start bit
Double word program	MCR.PGM	Address and data by interlock writes	MCR.EHV
Sector erase	MCR.ERS	LMS, HBS	MCR.EHV
Array integrity check	None	LMS, HBS	UT0.AIE
Margin read	UT0.MRE	UT0.MRV + LMS, HBS	UT0.AIE
ECC logic check	UT0.EIE	UT0.DSI, UT1, UT2	UT0.AIE

In general each modify operation is completed through a sequence of four steps:

1. Wait for operation completion: wait for bit MCR.DONE (or UT0.AID) to go high.
2. Check operation result: check bit MCR.PEG (or compare UMISR0-4 with expected value).
3. Switch off FPEC by resetting MCR.EHV (or UT0.AIE).
4. Deselect current operation by clearing MCR.PGM/ERS (or UT0.MRE/EIE).

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Static RAM

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SRAM Features

The SRAM provides the following features:

- SRAM can be read/written from any bus master
- Byte, halfword and word addressable
- ECC (error correction code) protected with single-bit correction and double-bit detection
- Except in standby mode, all SRAM is powered on.
- While in standby mode, user can decide to either power on all 48k or just 8k SRAM for power saving purpose.

Table 18-1. Low power configuration

Mode	Configuration
RUN, TEST, SAFE and STOP	The entire SRAM is powered and operational.
STANDBY	Either all or just 8 KB of the SRAM remains powered. This option is software-selectable.

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MPU

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MPU Block Diagram and Features

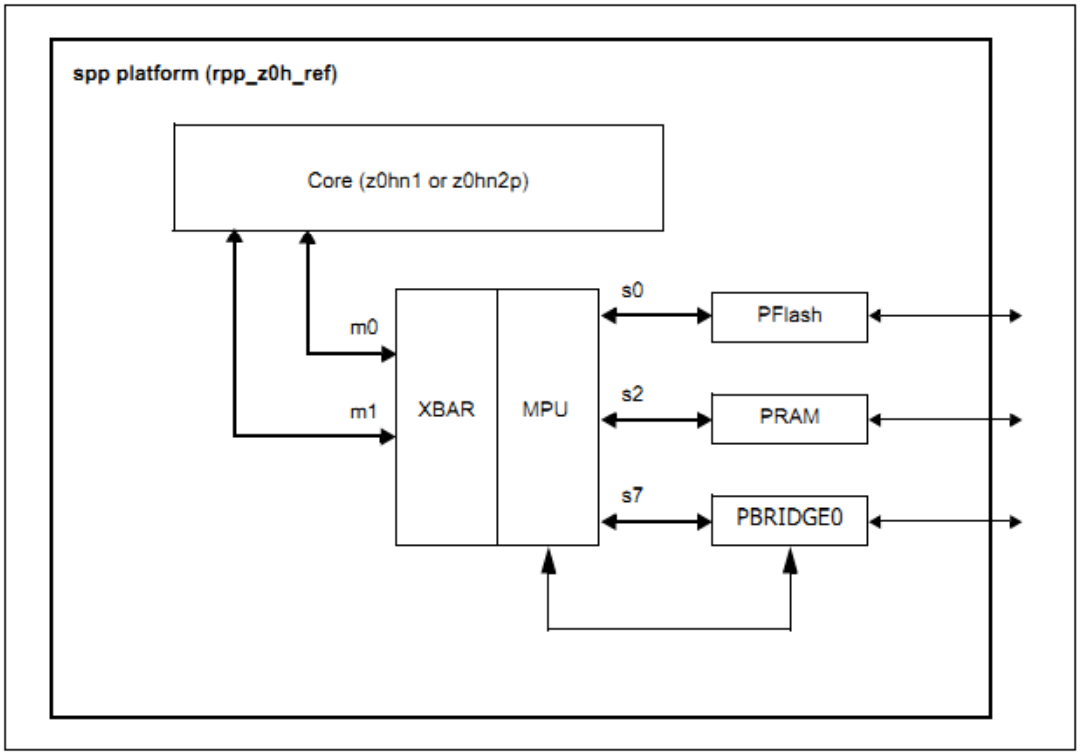

Figure 14-1. MPU block diagram

Features

❖ MPU provides hardware access control for all memory references generated in the device.

❖ Support for 8 program-visible 128-bit region descriptors.

❖ Support for 3 AHB slave port connections: flash controller, system RAM controller and IPS peripherals bus.

❖ Global MPU enable/disable control bit provides a mechanism to easily load region descriptors during system startup or allow complete access rights during debug with the module disable.

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ECC

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Concept of ECC

- ECC is the abbreviation of Error Correction Code.
- The objective of ECC is to enhance the reliability of data retention in the memory, either Flash or SRAM.
- ECC is a code corresponding to a set of data store in memory which contains the information relevant to that data.

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Flash ECC Mechanism

◆ For Flash memory, the 8-bit ECC code are always applied to a fixed size of 64-bit data.

◆ The 8-bit ECC code is capable of Single Error Correction and Double Error Detection, which in short is SEC-DED.

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SRAM ECC Mechanism

The SRAM ECC detects the following conditions and produces the following results:

- Detects and corrects all 1-bit errors
- Detects and flags all 2-bit errors as non-correctable errors
- Detects 39-bit reads (32-bit data bus plus the 7-bit ECC) that return all zeros or all ones, asserts an error indicator on the bus cycle, and sets the error flag

SRAM does not detect all errors greater than 2 bits.

ECC checks are performed during the read portion of an SRAM ECC read/write (R/W) operation, and ECC calculations are performed during the write portion of a R/W operation. Because the ECC bits can contain random data after the device is powered on, the SRAM must be initialized by executing 32-bit write operations prior to any read accesses. This is also true for implicit read accesses caused by any write accesses of less than 32 bits as discussed in Section 17.4, "SRAM ECC mechanism.

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ECC Interrupt

IRQ #	Offset	Size (bytes)	Interrupt	Module
33	0x0884	4	Match on channel 3	STM
34	0x0888	4	Reserved	
35	0x088C	4	ECC_DBD_PlatformFlash | ECC_DBD_PlatformRAM	Platform ECC Double Bit Detection
36	0x0890	4	ECC_SBC_PlatformFlash | ECC_SBC_PlatformRAM	Platform ECC Single Bit Correction

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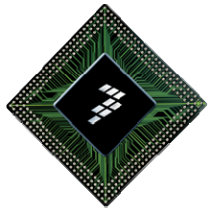

6. Interrupt Control

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Overview of Instruction Control

- ***e200z0 Interrupt control mechanism is defined by a Power Architecture Book-E ISA.***
- ***The implementation of the mechanism is called INTC module in MPC560x MCU.***

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Interrupts: e200z0 Interrupt Vectors

IVOR #	Interrupt Type	Enables[1]	State Saved In	Examples
IVOR0	Critical Input	CE	CSRR0:1	Non-maskable interrupt (pins PD[10], PD[11])
IVOR1	Machine Check	ME	CSRR0:1	ISI, ITLB error on 1st instr'n of exception handler
IVOR2	Data Storage	-	SRR0:1	Incorrect privilege mode for R/W access
IVOR3	Instruction Storage	-	SRR0:1	Incorrect privilege mode for instruction
IVOR4	External Input	EE, src	SRR0:1	Peripherals, IRQ pins, software
IVOR5	Alignment	-	SRR0:1	Load or store operand not word aligned
IVOR6	Program	-	SRR0:1	Illegal instruction, trap
IVOR7[2]	FP Unavailable	-	SRR0:1	FP instruction attempt with MSR[FP]=0
IVOR8	System Call	-	SRR0:1	System call, "sc", instruction
IVOR10[2]	Decrementer	EE, DIE	SRR0:1	Decrementer timeout
IVOR11[2]	Fixed-Interval Timer	EE, FIE	SRR0:1	Fixed-interval timer timeout
IVOR12[2]	Watchdog Timer	CE, WIE	CSRR0:1	Watchdog timeout when ENW=1, WIS=0
IVOR13[2]	Data TLB Error	-	SRR0:1	Data TLB miss in MMU
IVOR14[2]	Instruct'n TLB Error	-	SRR0:1	Instruction TLB miss in MMU
IVOR15	Debug	DE, IDM	CSSR0:1	ROM Debugger when HID0[DAPUEN]=0
		DE, IDM	DSRR0:1	ROM Debugger when HID0[DAPUEN]=1

1 CE, ME, EE, DE are in MSR. DIE, FIE, WIE are in TCR. "src" is individual enable for each INTC source. Debug interrupt, IVOR15, also requires EDM = 0 (EDM and IDM are in DBCR0).

2 Unused on e200z0

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Interrupts: Hardware and Software Vector Mode

Software Vector Mode

- The CPU branches to one of the 16 core interrupt vectors (IVOR's) which contains a branch to an exception handler (eg IVOR4 handler)
- The exception handler is common for the majority of exceptions
  - Prologue
  - Identification of specific interrupt by reading a register
  - Location of ISR is read from a jump table
  - Branch to ISR
  - Common epilogue

Note – Hardware and software vector mode are only relevant to IVOR4 (INTC) exceptions

Hardware Vector Mode

- The IVOR4 vector is not used, instead each interrupt has a unique vector entry containing the jump address of the ISR. The ISR contains:
  - Unique Prologue
  - ISR
  - Unique Epilogue

HW and SW Vector Modes are configurable by core (in **INTC_MCR**), so one core can use SW Vector Mode, and the other HW Vector Mode

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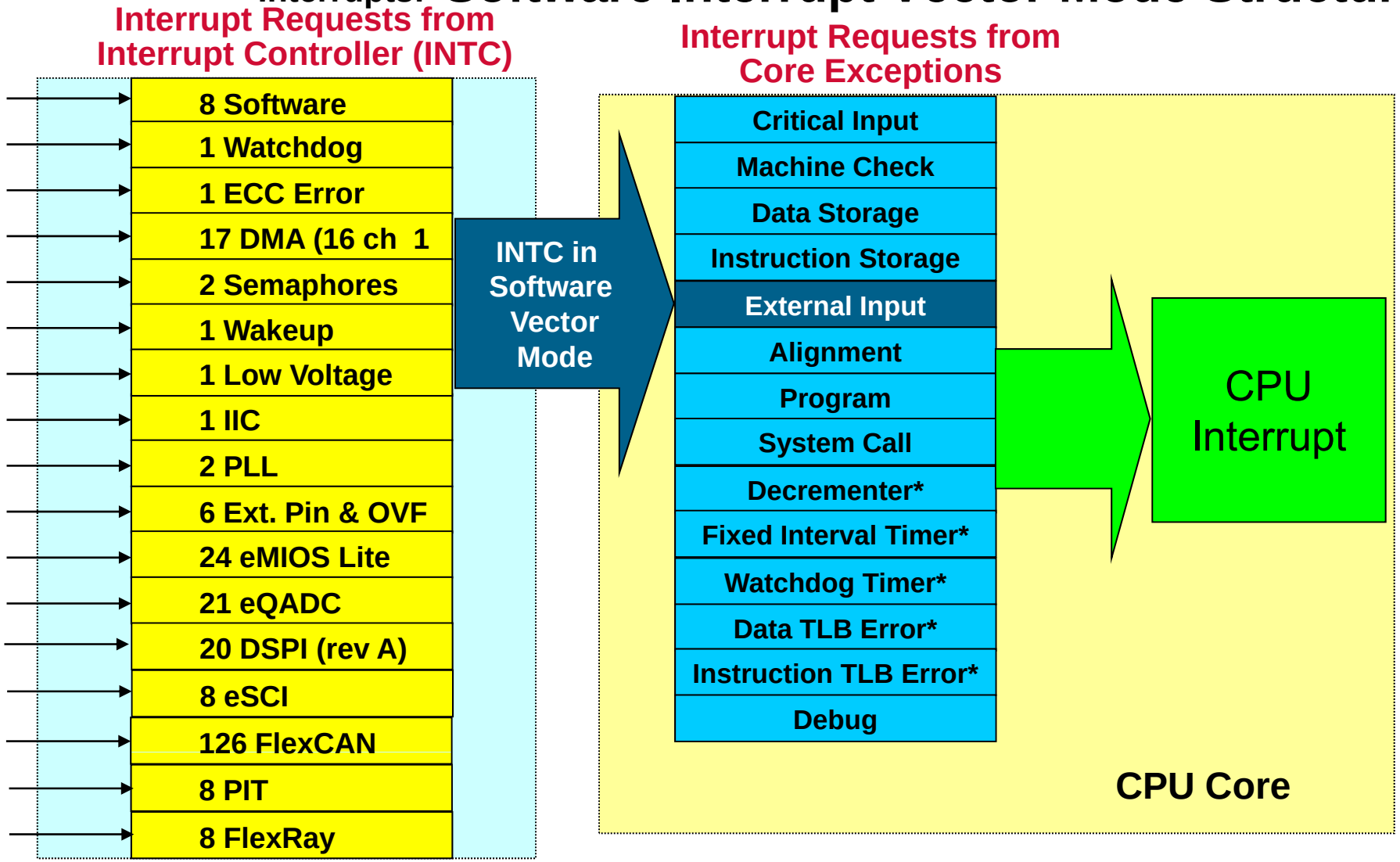
Interrupts: Software Interrupt Vector Mode Structure



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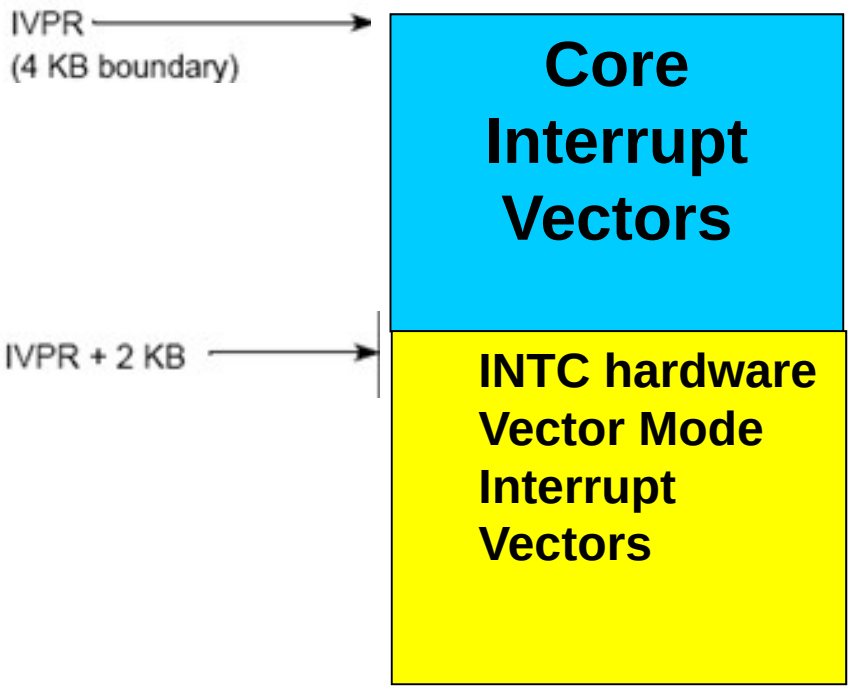
Interrupts: Hardware Interrupt Vector Mode Structure

The interrupt vectors are located on a 4KByte boundary.

- Hardware vector mode has IVPR (Interrupt Vector Prefix Register) at a 2Kbyte offset from the software mode IVPR



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Interrupts: Software Vector Mode Interrupt Handler

The IVOR4 Interrupt handler consists of 3 main parts:

Prologue

- Save SRR's to stack
- Read **IACKR** to determine which INTC interrupt occurred (See next slide)
- Re-enable interrupts in MSR
- Save GPR's to stack

Jump to ISR

- Branch with link to IACKR

Epilogue

- Execute mbar to ensure all pending data operations are complete before restoring any registers!
- Write to EOIR (Sets CPR back to previous value)
- Restore GPR's
- Disable Interrupts in MSR
- Restore SRR's
- Execute RFI (Return to address in SRR0 and restore MSR)

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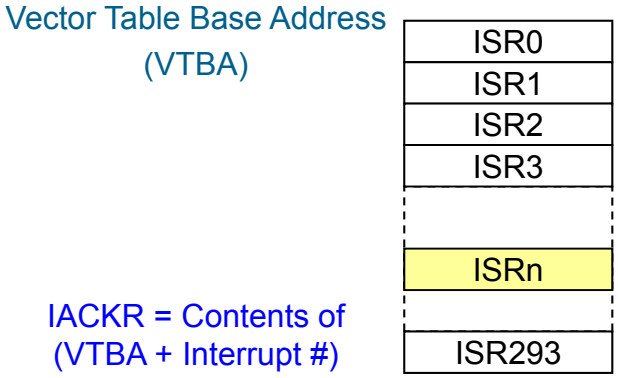
INTC: Software Vector Mode Interrupt Acknowledge

Each core has an Interrupt Acknowledge Register (IACKR) valid for IVOR4 (INTC) exceptions in software vector mode.

- **INCT_IACKR_PCR0 / INCT_IACKR_PCR1**
- Reading this register acknowledges the interrupt has taken place and prevents the same interrupt occurring again
- Reading IACKR also calculates and returns the address of the relevant Interrupt Service Routine based on reading the 32-bit address at “VTBA + ISR Offset”



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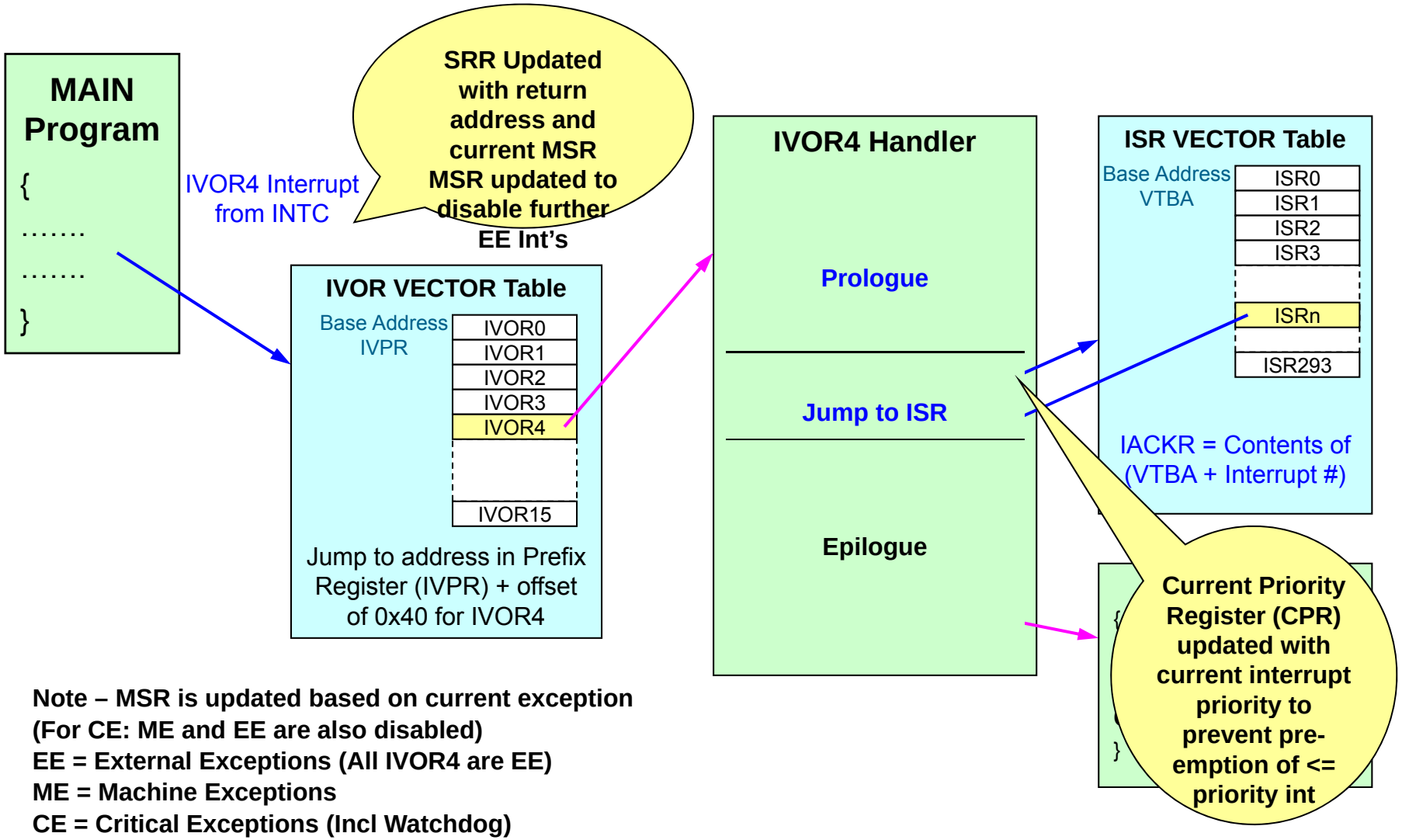
INTC: Software INTC Interrupt Example



Note – MSR is updated based on current exception (For CE: ME and EE are also disabled)
EE = External Exceptions (All IVOR4 are EE)
ME = Machine Exceptions
CE = Critical Exceptions (Incl Watchdog)

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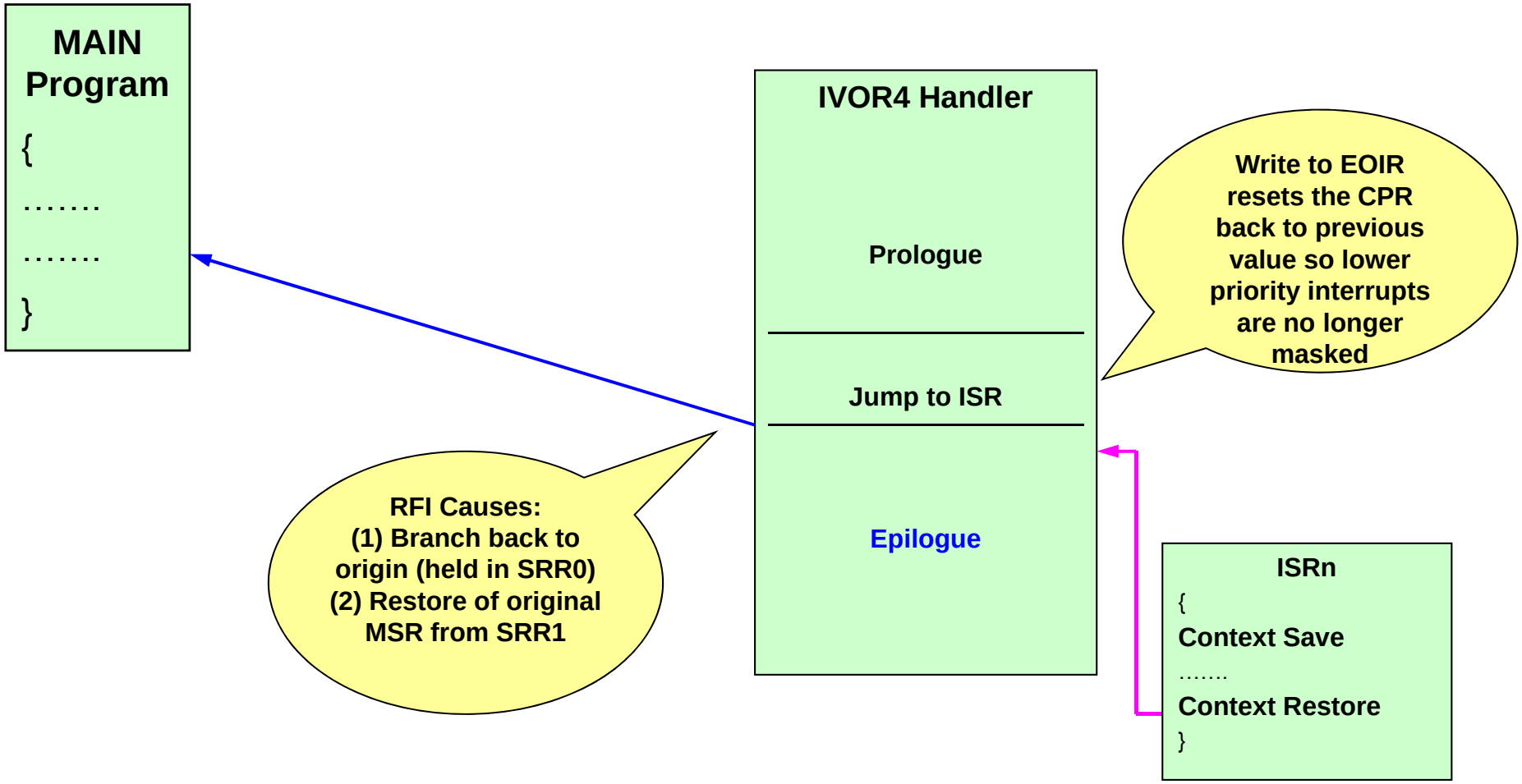
INTC: Software INTC Interrupt Example



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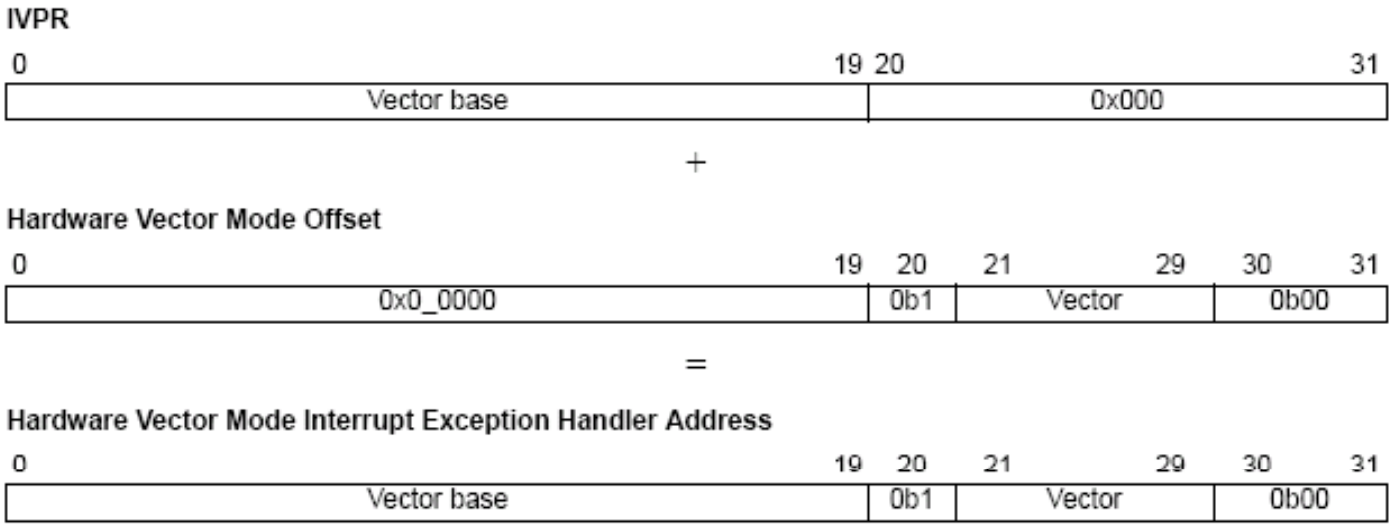
INTC: Hardware Vector Mode Details

In hardware vector mode, IVOR4 is not used!

- Each INTC interrupt has a unique 4 byte vector entry in the vector table at IVPR+2KB
- The table entry is calculated by adding the 4 byte vector to the IVPR
- There is no common handler and each interrupt ISR has it's own prologue and epilogue



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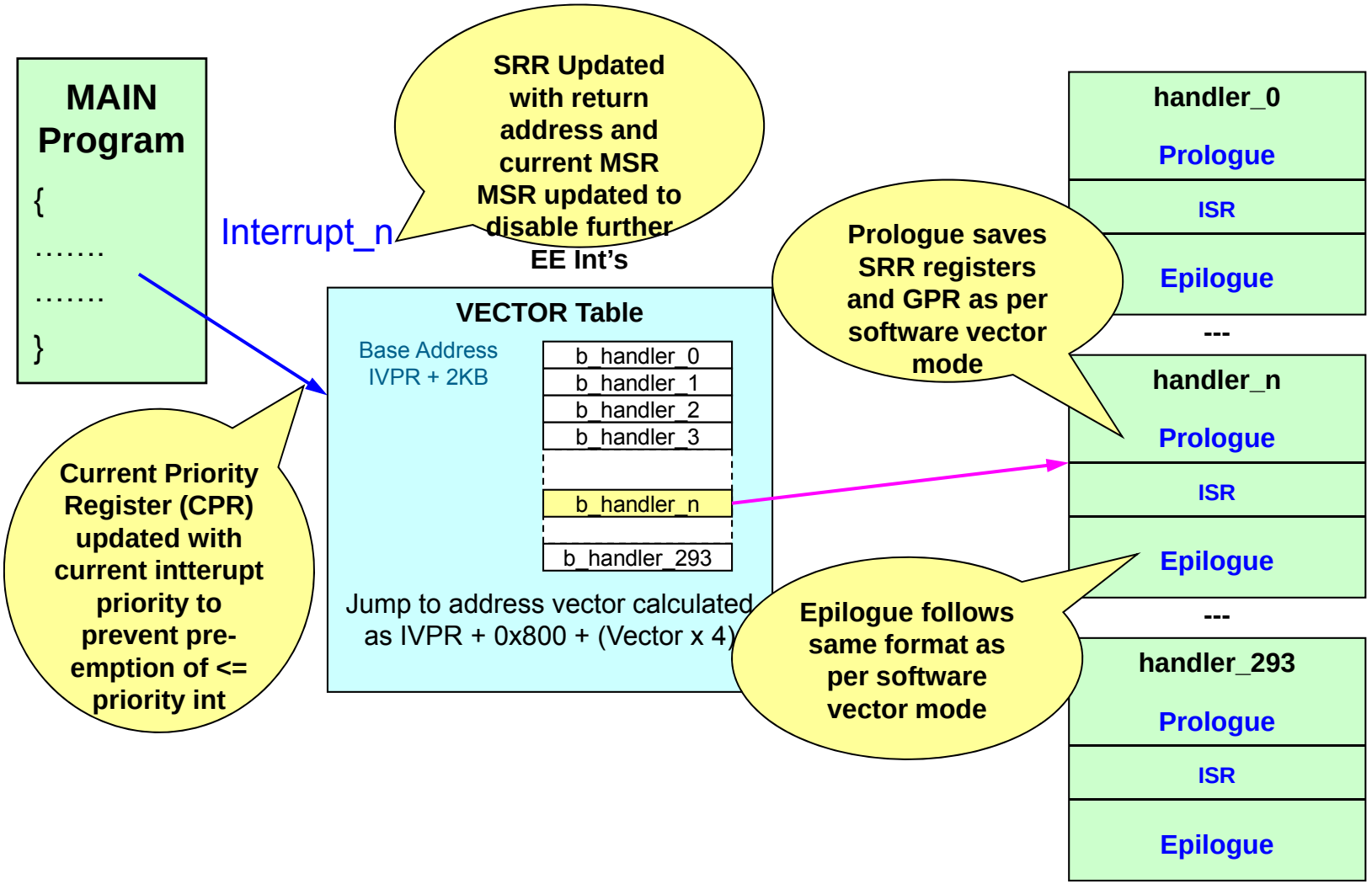
INTC: Hardware Interrupt Example



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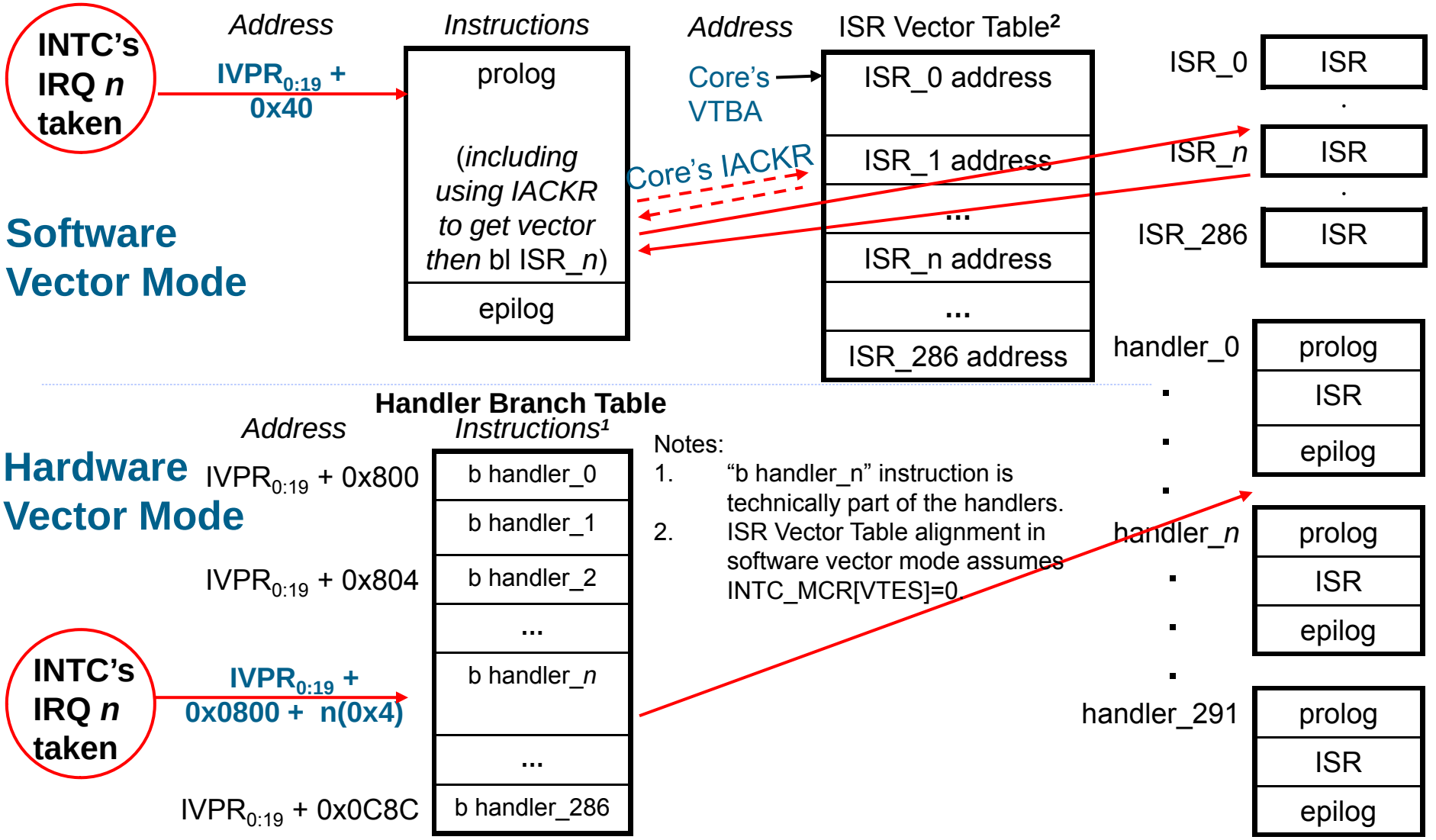
INTC: MPC560xB Software & Hardware Vector Modes



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INTC: SW vs HW Vector Mode Handler

Software Vector Mode *(HVEN = 0)*	Hardware Vector Mode *(HVEN = 1)*
HW: - Backs up machine state to SRR0:1 - Disables interrupts except CE, ME, DE **- Takes External Input Interrupt based on IVPR and offset 0x40 (for "IVOR4")**	HW: - Backs up machine state to SRR0:1 - Disables interrupts except CE, ME, DE **- Takes unique IRQ vector based on IVPR and offset which matches INTVEC**
SW Prolog: - Saves SRR0:1* **- Reads INTC_IACKR[INTVEC]** - Re-enables MSR[EE]* - Saves other registers	SW Prolog: - Saves SRR0:1* - Re-enables MSR[EE]* - Saves other registers
SW: **- branches per INTC_IACKR[INTVEC]**	
SW ISR (clears interrupt flag)	SW ISR (clears interrupt flag)
SW Epilog: - Executes *mbar* to ensure IRQ flag cleared - Restores most registers - Disables EE* and writes to INTC_EOIR - Restores remaining registers and returns (rfi)	SW Epilog: - Executes *mbar* to ensure IRQ flag cleared - Restores most registers - Disables EE* and writes to INTC_EOIR - Restores remaining registers and returns (rfi)

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What are the advantages / disadvantages of HW and SW interrupts?

Software

- Conforms to Power Architecture (minor point)
- Common IVOR handler for 294 ISR's saves code.
- More convoluted than hardware

Hardware

- Faster than software to execute
- Inherently simpler to code / understand than software
- Less code efficient with prologue and epilogue in each handler!

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INTC: Software Interrupts

Eight interrupt vectors are assigned to software interrupts

- Software interrupts 0:7 have interrupt vectors 0:7

A software interrupt request is triggered by software writing a ‘1’ to a SET***x*** bit in INTC Software Set/Clear Interrupt Registers **(INTC_SSCIR[0:7])**

A software interrupt request is cleared by software writing a ‘1’ to a CLR***x*** bit in INTC Software Set/Clear Interrupt Registers

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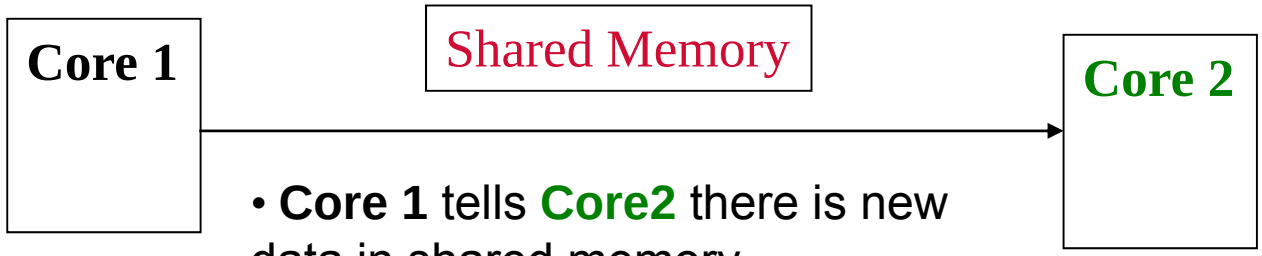
Scheduling lower priority portions of an ISR

Without SW IRQ

- ISR partitioned into two ISRs.
- Setting software interrupt in higher priority portion requests lower priority portion to complete at a later time.

- Interprocessor Communication



- **Core 1** tells **Core2** there is new data in shared memory.

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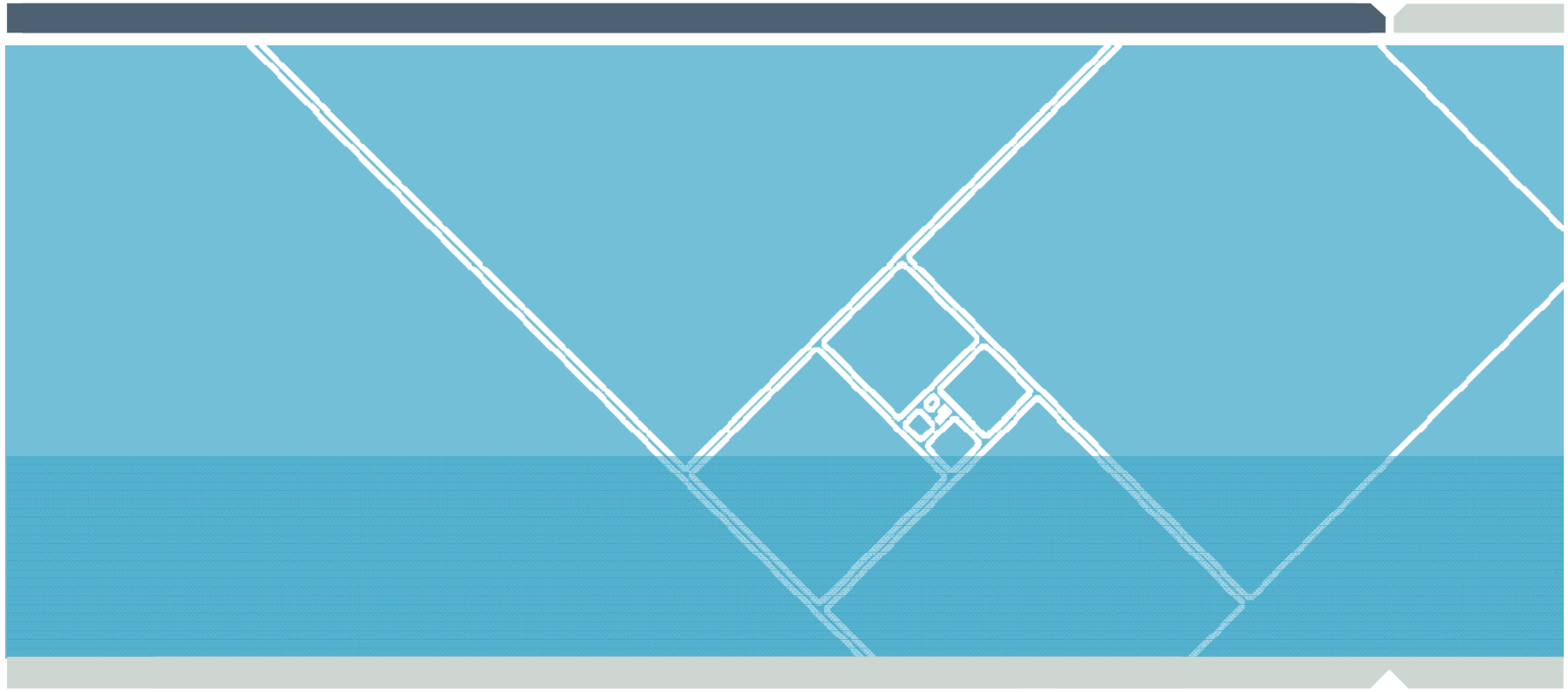

7. Communication Modules

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Communication Modules

- ***DSPI***
- ***LINFlex***
- ***FlexCAN***
- ***IIC***

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DSPI

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DSPI: Features

High speed, full duplex, three wire synchronous interface
Master and slave modes supported
Six Peripheral Chip Selects
- Expandable to 64 with external demultiplexer
- Deglitching support of up to 32 chip selects when external mux used

SPI Queue support
- Buffered transfers using 4 deep Tx FIFO and 4 deep Rx FIFO
- FIFO visibility for debugging

6 Interrupt conditions

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DSPI: ConfigurationS

Serial Peripheral Interface (SPI) Configuration

- Operation as basic SPI or Queued SPI using internal FIFOs
- Programmable transfer attributes on a per frame basis
  - Serial clock: baud rate, polarity and phase
  - Frame size: 4 to 16 bits
  - Various programmable delays
  - Chip Select: Up to 6, and continuous hold capability

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DSPI: Configurations Block Diagram

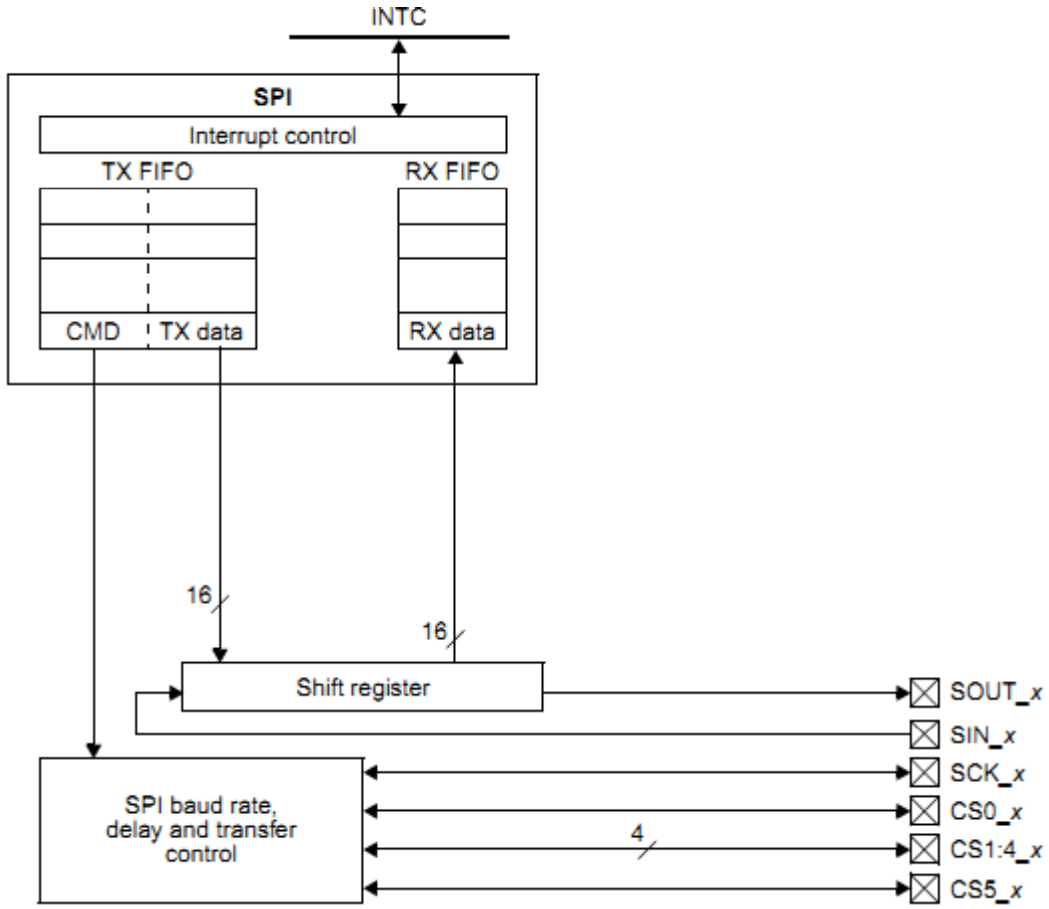

Figure 20-1. DSPI block diagram

DSPI Configuration of SPIis specified in DSPI_MCR[DCONF]

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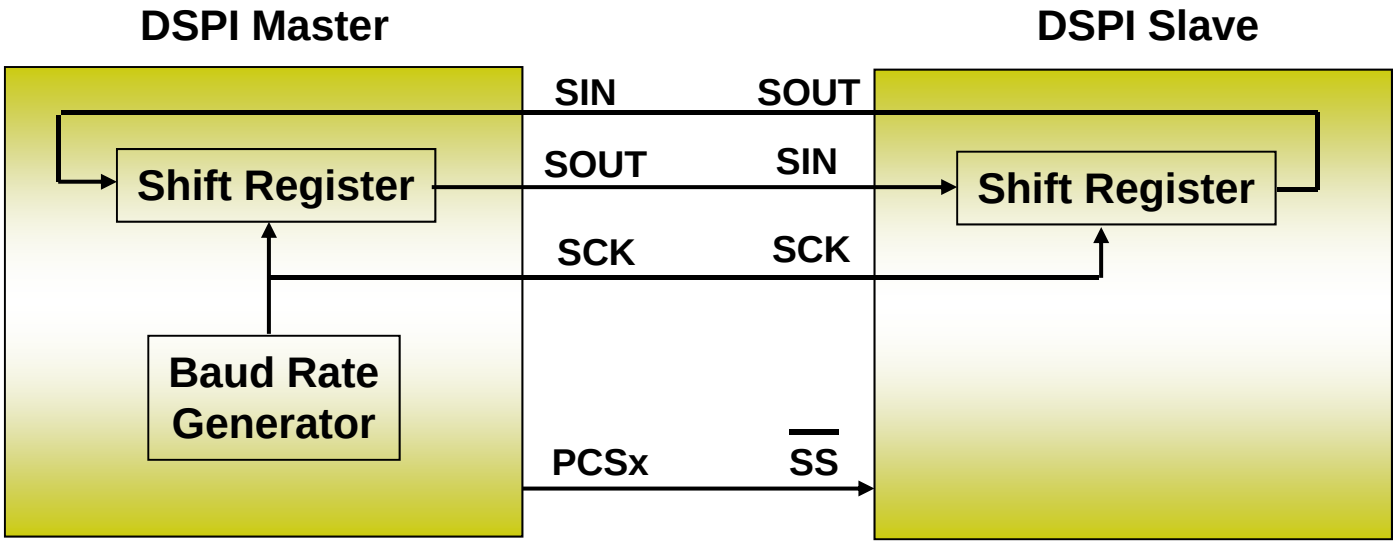
DSPI: Configuration of Master / Slave Mode

Selection of Master or Slave Mode is made in the DSPI_MCR[MSTR] bitfield

0: Slave (default)

1: Master



Note: PCSx to $\overline{SS}$ signal must be configured active low for slave mode operation.

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LINFlex

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LINFlex

Features:

- Supports LIN protocol version 1.3, 2.0, 2.1 and J2602
- UART mode
  - 7/8-bit data, parity/no-parity, 1 or 2 stop bit
  - LSB first

LIN Management

- Initialisation, Normal and Sleep
- Maskable interrupts
- Wake-up event on dominant bit detection
- 8-bit counter for time-out management
- Software-efficient data buffer interface mapping at a unique address space

LIN Master Mode

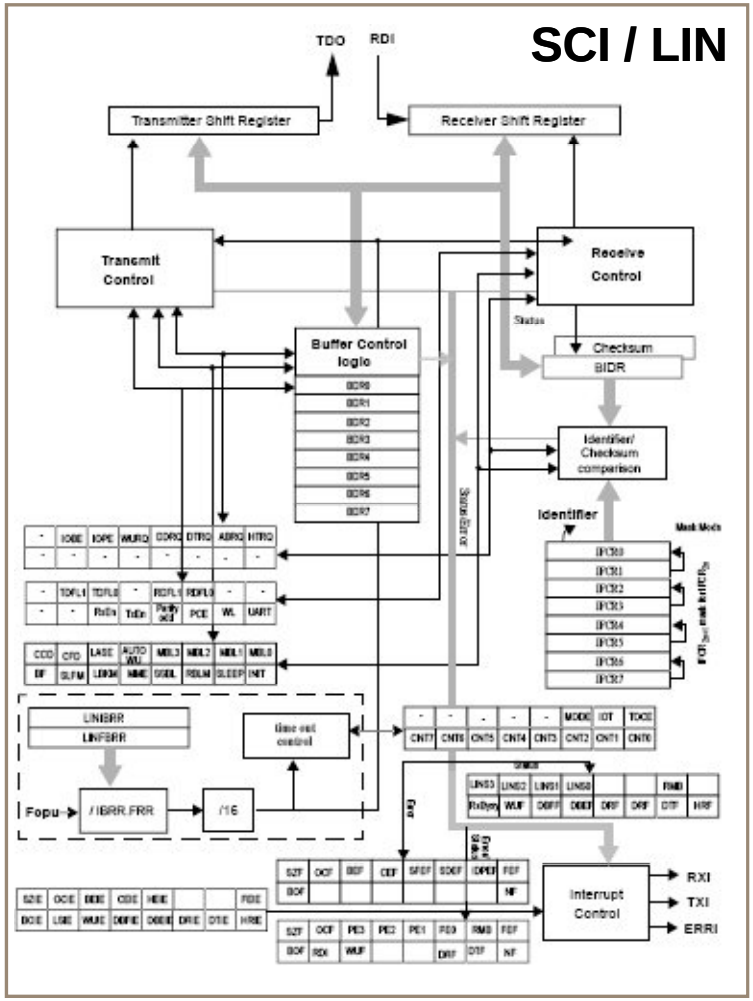
- Autonomous message handling
- Once the software has triggered the header transmission, no further intervention needed:
  - until the next header transmission request in transmission mode
  - until the checksum reception in reception mode

LIN Slave Mode (only LINFlex0 on Bolero is capable of slave mode)

- Software intervention needed only to:
  - Trigger transmission, reception or discard depending on the identifier,
  - Fill the buffer (transmission) or get data from buffer (reception).
- In Filter mode Software intervention needed only to:
  - Fill the buffer in transmission,
  - Get data from buffer in reception.
  - If Filter mode is combined with DMA (one channel per filter), no software intervention required

UART mode

- Full duplex; Character length 7 & 8 bits; opt parity, 1 or 2 stop bits
- 4 byte Tx and Rx buffers
- 3 interrupt sources : error, Rx, Tx
- LSB first



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LINFLEX
Operating modes

Initialization mode:

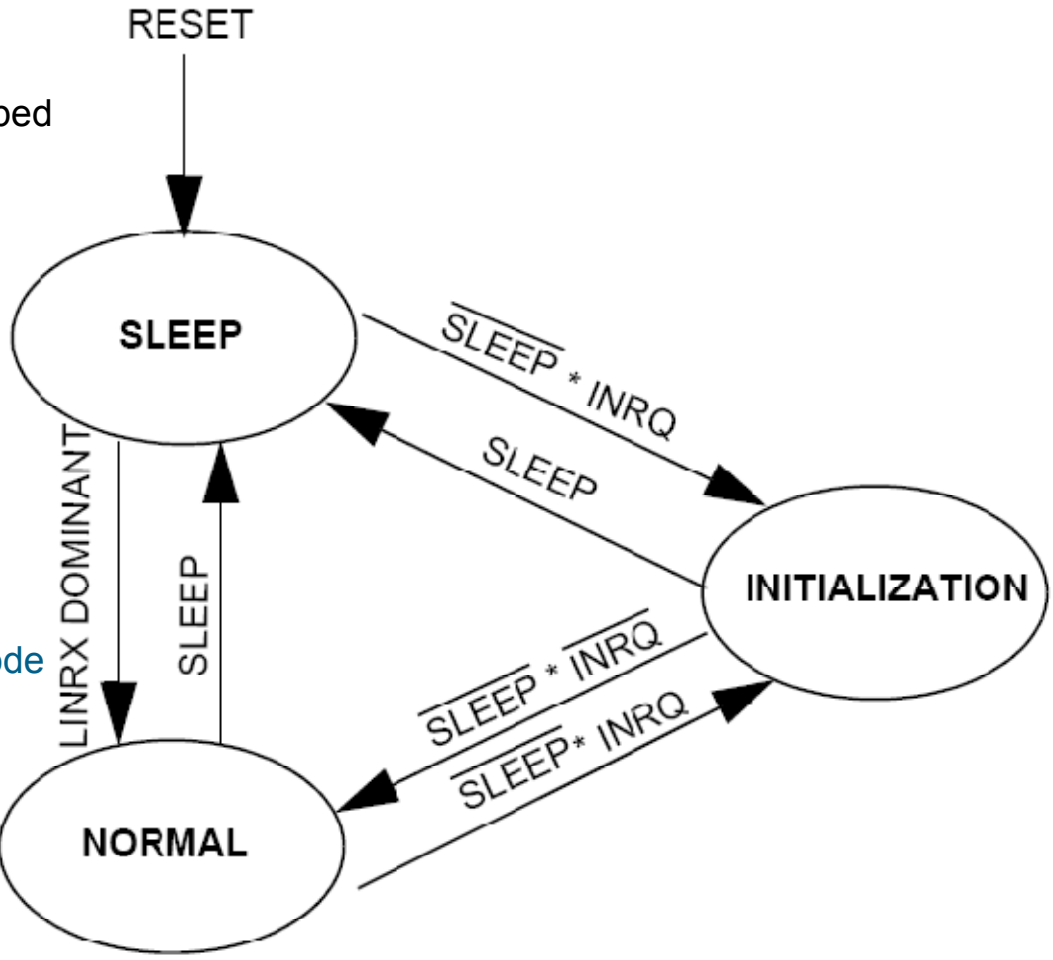
- all transfers to and from the LIN bus are stopped
- LIN TX Pin is recessive (high)
- Entering INIT mode does not change the configuration registers
- LIN and UART configuration registers can only be written in INIT mode

Normal mode:

- Main user mode
- Configuration registers protection in RUN mode

Sleep mode:

- low power mode entered on SW request
- LINFlex clock stopped,
- exit possible by SW or HW



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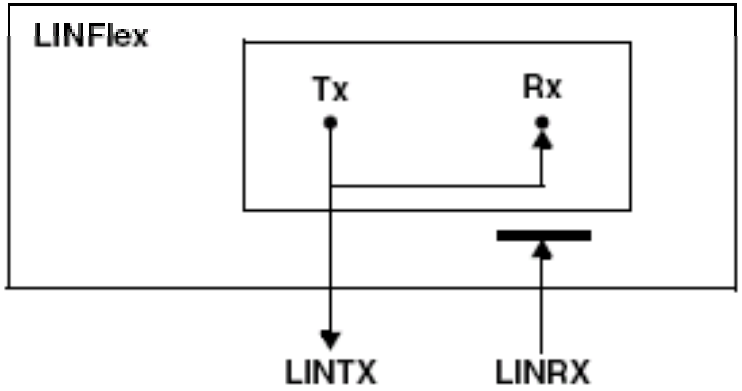
LINFLEX
Test modes

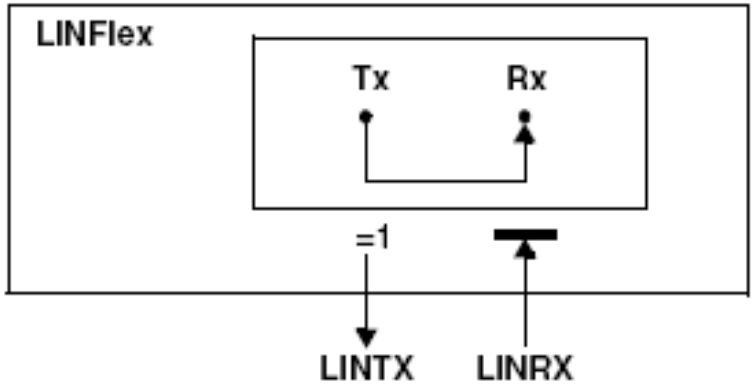
Loopback:

- Self-test mode
- LINFlex treats transmitted messages as received messages to be independent of external events



Selftest:

- hot self-test mode
- like loopback mode, but without affecting the running system



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LINFLEX
Enhanced error detection circuit

Bit error

- Detection on all bits transmitted including header, delimiters

Identifier Parity

Break Delimiter

Inconsistent Synch Field

Framing error

Checksum Error

- Classic
- Enhanced

- Slave response timeout
  - Dedicated timer programmable by application
- LINRX stuck dominant
- Buffer overrun
- Error signalling in LINESR register
  - 9 error sources
  - Each error source can be independently enabled/disabled

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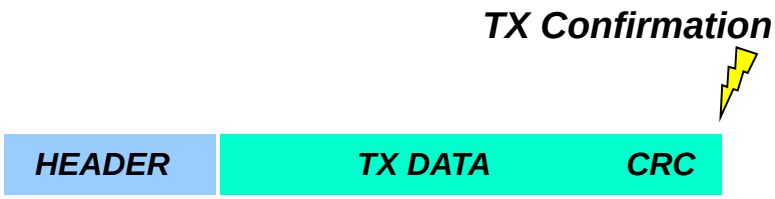
LINFLEX Overview

Protocol handler - Master mode

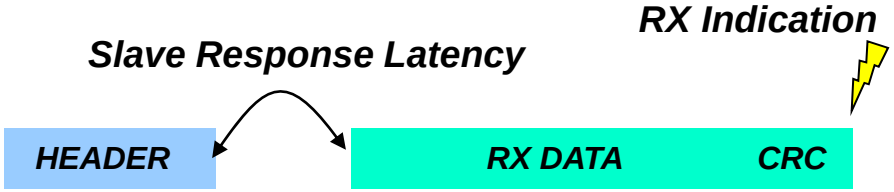
Header and response handling without CPU intervention

Master as publisher:

- Software configures ID, Data length, direction, fill Data Buffer and request transmission
- Transmission without dead-time
- Synch Break length configurable from 10 to 36 bit times (COOLING, i.e. proprietary protocol for LIN)
- Checksum calculated automatically



TRANSMIT RESPONSE



RECEIVE RESPONSE

Master as subscriber:

- Software configures ID, Data length, direction, and request transmission
- Reception indication

IGNORE RESPONSE

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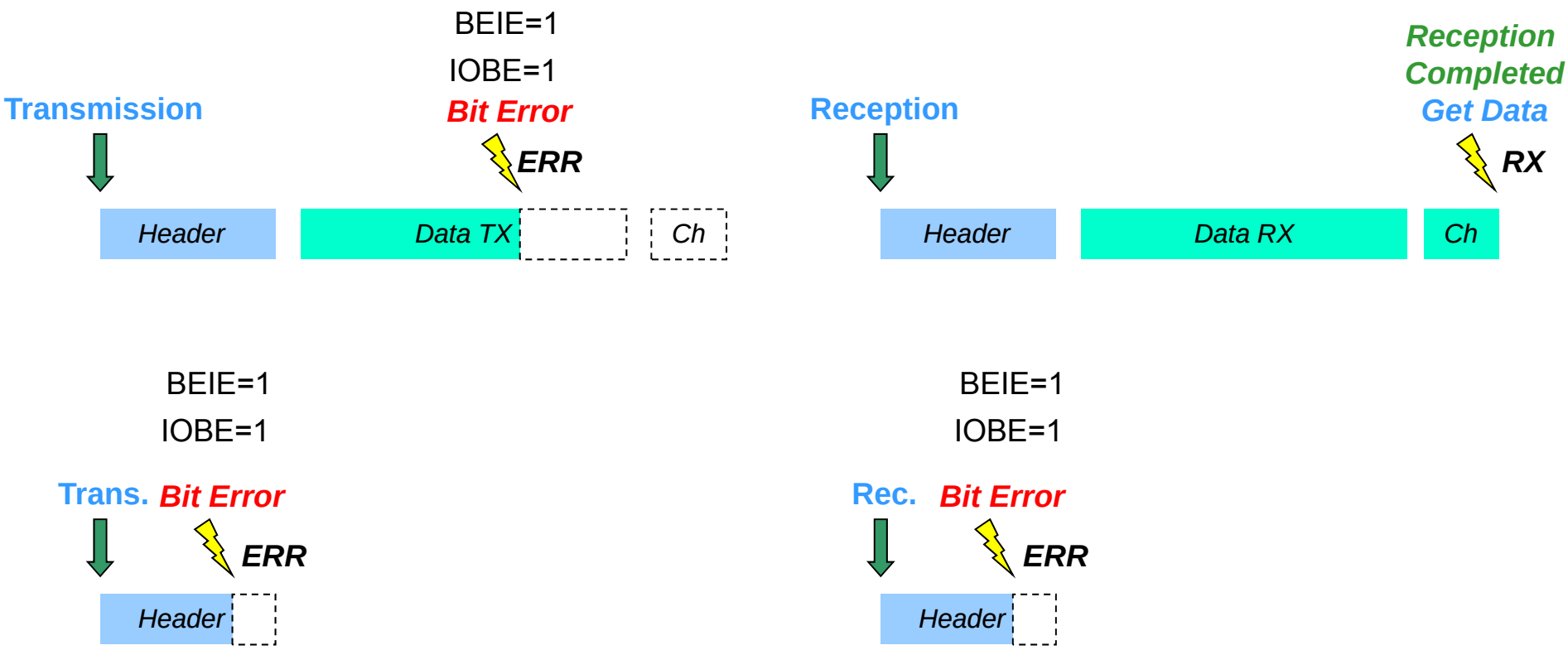
LINFLEX
Master mode – bit error (idle on bit error enable)

value read back from the bus differs from the from the transmitted value



Communication stopped immediately

Interrupt to notify bit error

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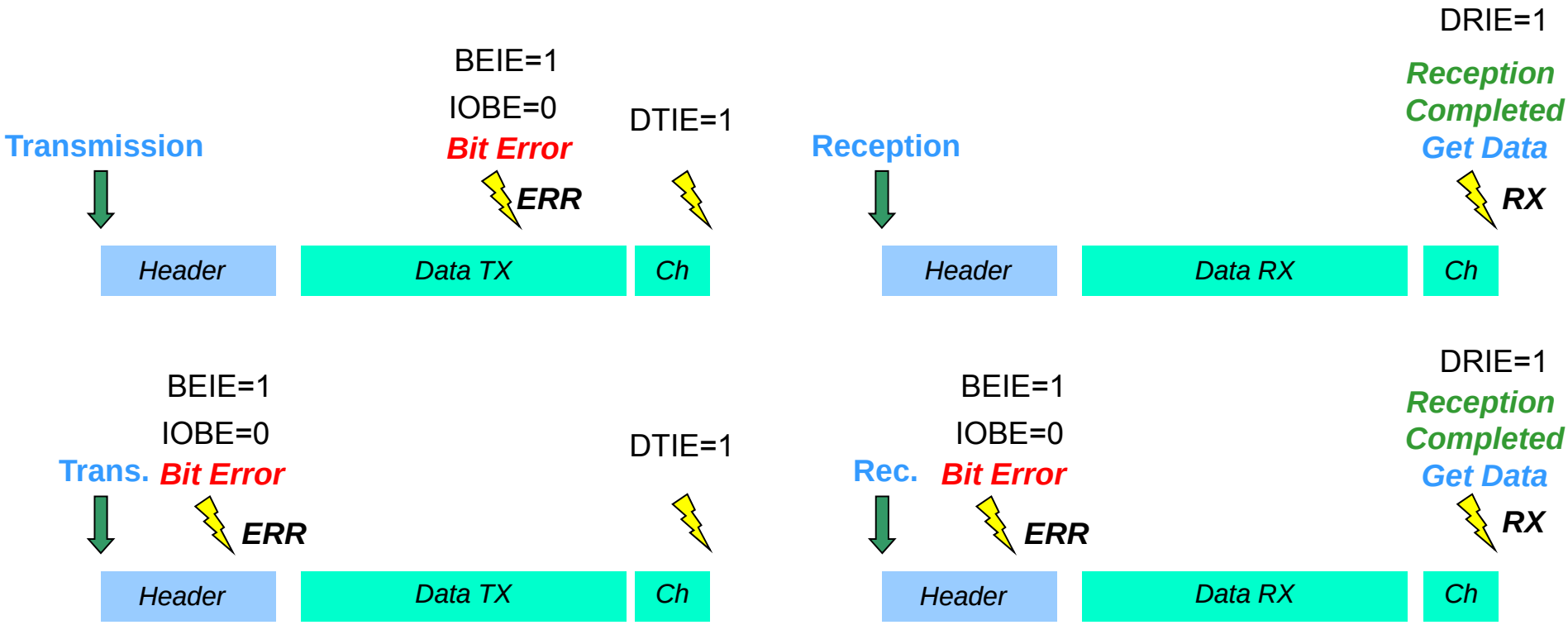
LINFLEX
Master mode – bit error (idle on bit error disable)



Software can take appropriate action on bit error interrupt

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LINFLEX Overview

Protocol Handler - Slave mode (only LINFlex0 on Bolero)

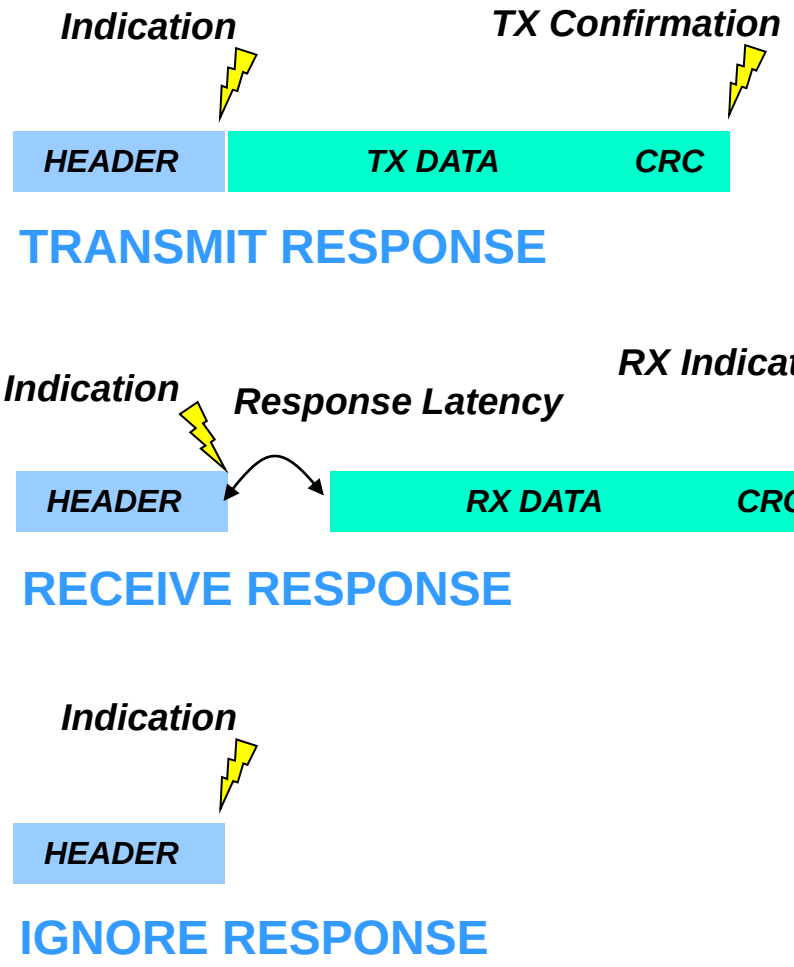
Header and response handling with minimum CPU intervention

Slave as publisher:

- Indication after reception of a correct identifier

Response

- Transmission confirmation
- Reception indication
- 8 optional identifier filters for automatic reception



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LINFLEX Overview

UART mode

Mode

- Full Duplex
- 8-bit / 9-bit
- Even / Odd parity

Transmit Buffer

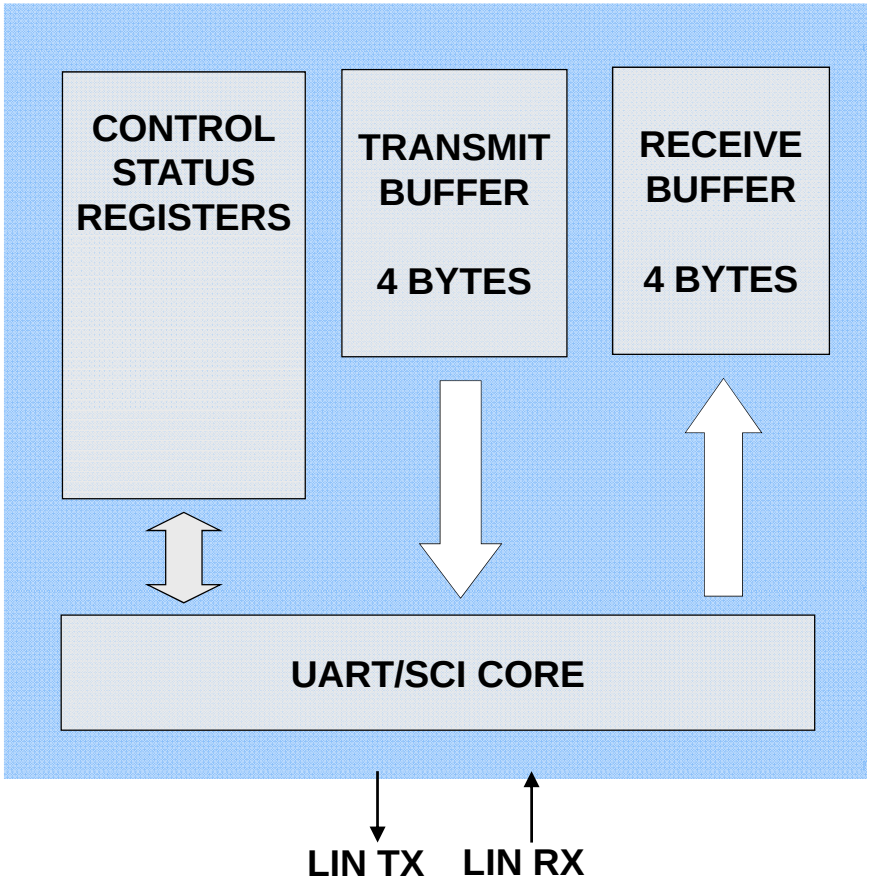
- Depth configurable from 1 to 4

Receive Buffer

- Depth configurable from 1 to 4

Error

- Parity
- Overrun



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FlexCAN

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FlexCAN Module Features:

- CAN module which supports both CAN A and CAN B specifications
- 64 message buffers per module
- Filters for receive message buffers
- Message buffers and errors can cause interrupts
- Programmable loop-back for self test operation
- Can wakeup on bus activity using FlexCAN input pins through CRP
  - Wakeup internal to FlexCAN is not supported

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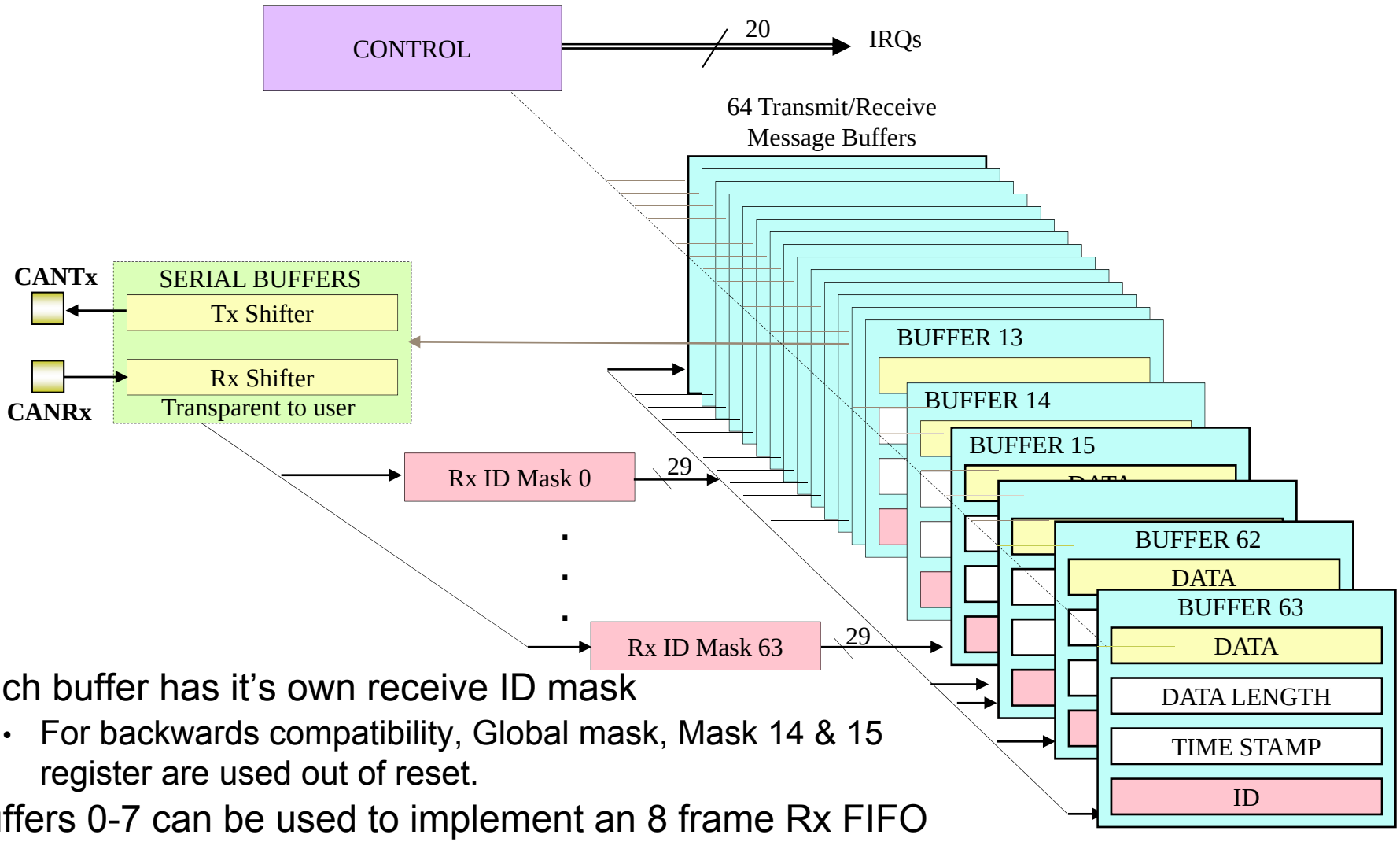
FlexCAN: Architecture with FlexCAN



Each buffer has it's own receive ID mask

- For backwards compatibility, Global mask, Mask 14 & 15 register are used out of reset.

Buffers 0-7 can be used to implement an 8 frame Rx FIFO

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FlexCAN: Message Buffer Structure

FlexCAN Message Buffer Structure

0x0	-	**CODE**	- SRR* IDE RTR	LENGTH	TIME STAMP
0x4	-	ID (Extended/Standard) |			ID (Extended) *
0x8	Data Byte 0		Data Byte 1	Data Byte 2	Data Byte 3
0xC	Data Byte 4		Data Byte 5	Data Byte 6	Data Byte 7

Receive Buffer Codes

Before	After	Description
0000	-	Buffer not active
0010	0010 / 0110	Buffer is Full/Overrun
0100	0010	Buffer Active & Empty
0110	0110	Overrun (2nd frame rec'd before CPU read 1st frame)
0101	0010	An empty buffer was filled
0011	0110	A full/overrun buf. was filled

Transmit Buffer Codes

Before	After	Description
1000	-	Buffer not ready to transmit
1100	1000	Tx buffer ready to transmit once
1100	0100	Remote frame will transfer and msg. buf. becomes Rx buf.
1010	1010	Data frame will transfer only as a response to remote frame
1110	1010	Data frame to transfer once then only as a response to frame, always

Before buffer codes: Host CPU writes commands **After** buffer codes: Reflects the status of that buffer.

* Fields ignored when using standard frames (IDE=0)

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Bit Error - Detected by a transmitter if the bit value received is different from the bit value transmitted.

Exceptions:- sending a recessive bit and receiving a dominant bit during the Arbitration Field or the Ack Slot, or during a Passive Error flag.

Stuff Error - Detected by a receiver if 6 consecutive bit values are received during a message field that should be encoded by bit stuffing.

CRC Error - Detected by a receiver if the CRC calculated by the receiver is different from the CRC received in the CRC Sequence field.

Form Error - Detected by a receiver if a fixed form bit field contains one or more illegal bits.

Acknowledge Error - Detected by a transmitter if it does not receive a dominant bit during the ACK Slot.

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FLEXCAN Interrupts

20 unique INTC vectors per FLEXCAN2 module:

- 18 channel vectors
  - 16 unique for buffers 0-15
  - 1 for buffers 16-31 (“OR’d” together)
  - 1 for buffers 32-63 (“OR’d” together)
- 1 bus off vector
- 1 error vector

Each buffer has its own:

- Interrupt enable bit (mask)
  - 0: Interrupt is disabled
  - 1: Interrupt is enabled
- Status flag bit

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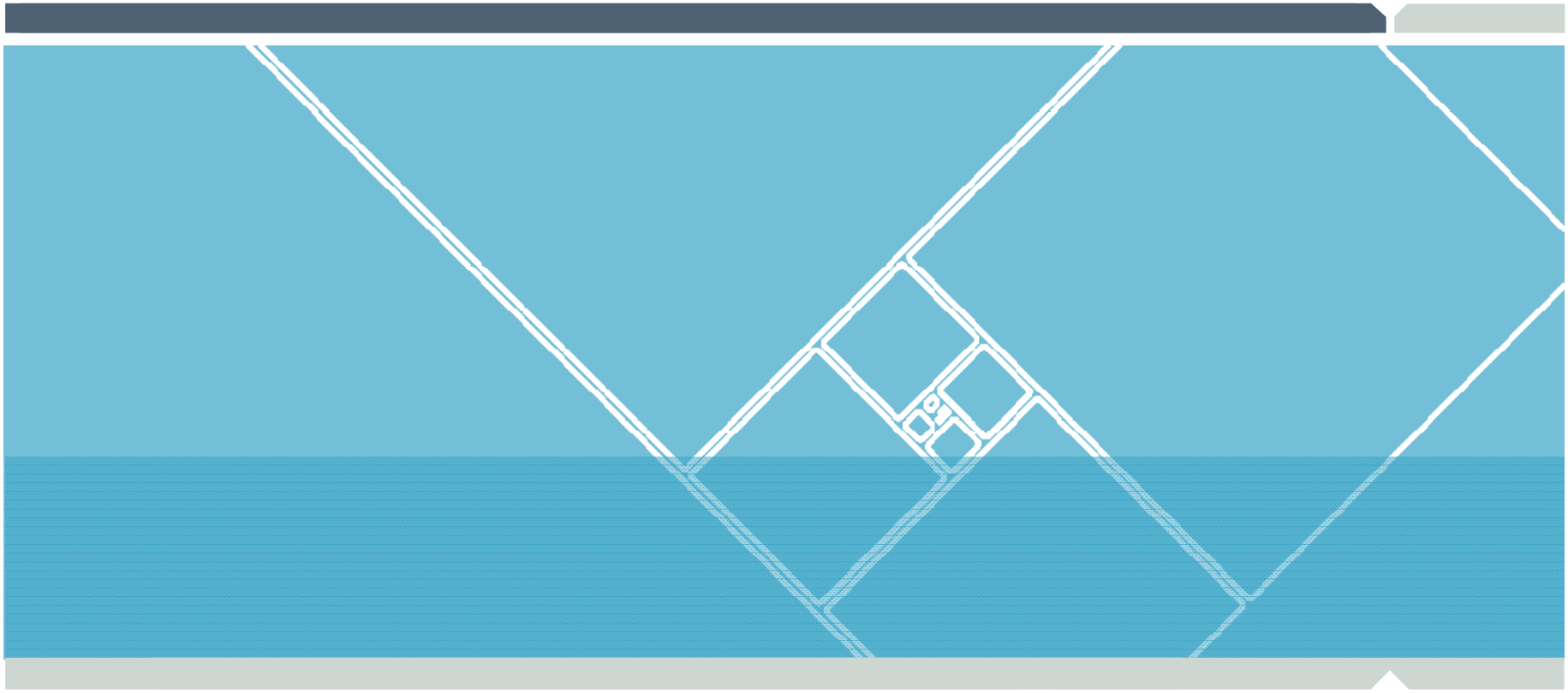

8. System Related

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System Related

- ***Peripheral Bridge***
- ***Crossbar Switch***
- ***BAM***

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Peripheral Bridge

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Peripheral Bridge

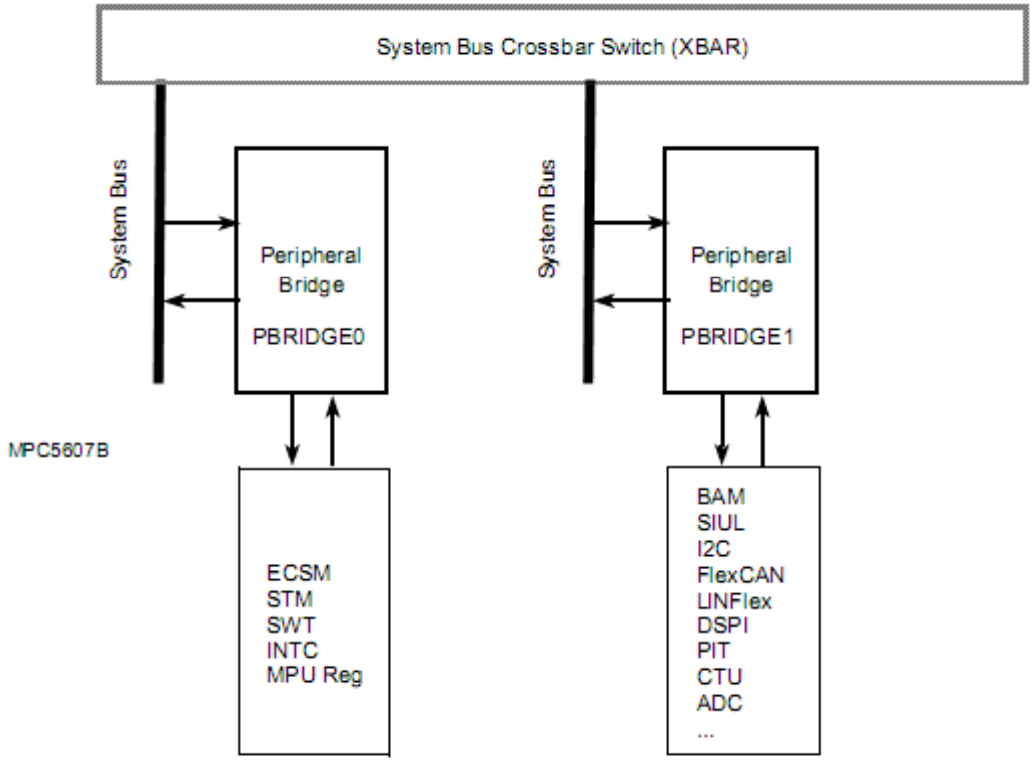

Figure 13-1. PBRIDGE Interface

- PBRIDGE is a interface between system BUS and on-chip peripherals.
- PBRIDGE on MPC560xB is a hard-wired implementation not software configurable.
- The PBRIDGE generates module enables, the module address, transfer attributes, byte enables, and write data as inputs to the slave peripherals.
- The PBRIDGE captures read data from the slave interface and drives it on the system bus.
- The PBRIDGE occupies a 64 MB portion of address space. The register maps of the slave peripherals are located on 16-KB boundaries.
- The PBRIDGE is responsible for indicating to slave peripherals if an access is in supervisor or user mode.

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Crossbar Switch

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Crossbar Switch (XBAR)

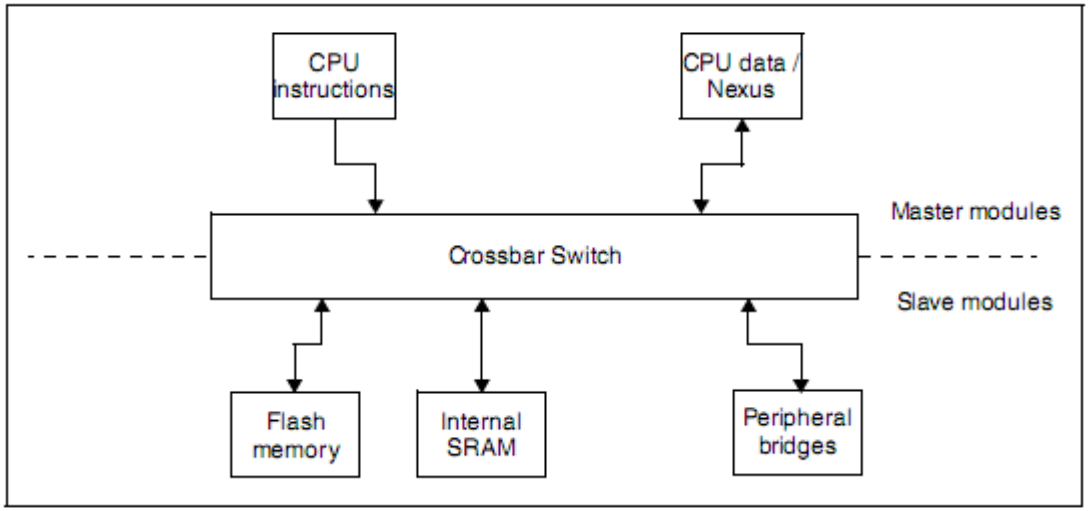

Figure 12-1. XBAR block diagram

Table 15-1. Master/Slave mappings

Module	Port		Physical master ID
	Type	Logical number	
e200z0 core—CPU instructions	Master	0	0
e200z0 core—CPU data / Nexus	Master	0	1
eDMA	Master	2	2
Flash	Slave	0	—
Internal SRAM	Slave	2	—
Peripheral bridge	Slave	7	—

- The purpose of the XBAR is to concurrently support up to eight simultaneous connections between master ports and slave ports.
- Each slave port can support multiple master priority schemes. Each slave port has a hardware input which selects the maser priority scheme so dynamically change master priority levels on slave port by slave port basis.
- XBAR supports a 32-bit address bus width and a 32-bit data bus width at all master and slave ports.

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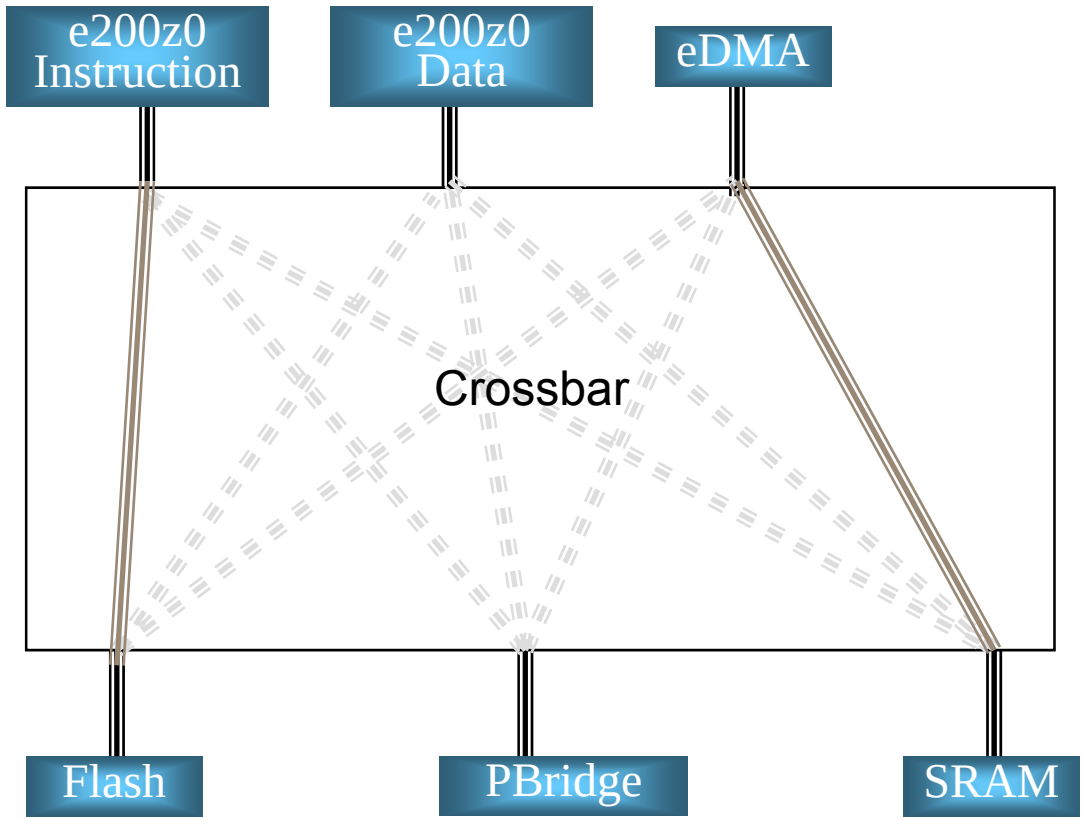
Arbitration



XBAR Structure of MPC5605B

- The XBAR supports two arbitration schemes; a simple fixed-priority comparison algorithm, and a simple round-robin fairness algorithm.
- The arbitration scheme is independently programmable for each slave port.
- When operating in fixed-priority mode, each master is assigned a unique priority level in the MPR and AMPR. If two masters both request access to a salve lport the master with the highest priority in the selected priority register will gain control over the slave port.
- When operating in round-robin mode, each master is assigned a relative priority based on the master number. This relative priority is compared to the ID of the last master to perform a transfer on the slave bus. The highest priority requesting master will become owner of the slae bus as the next transfer boundary.

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BAM

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Boot Mode Selection

Notes:

- The gray modules are done by hardware automatically.
- The white modules are done by BAM.

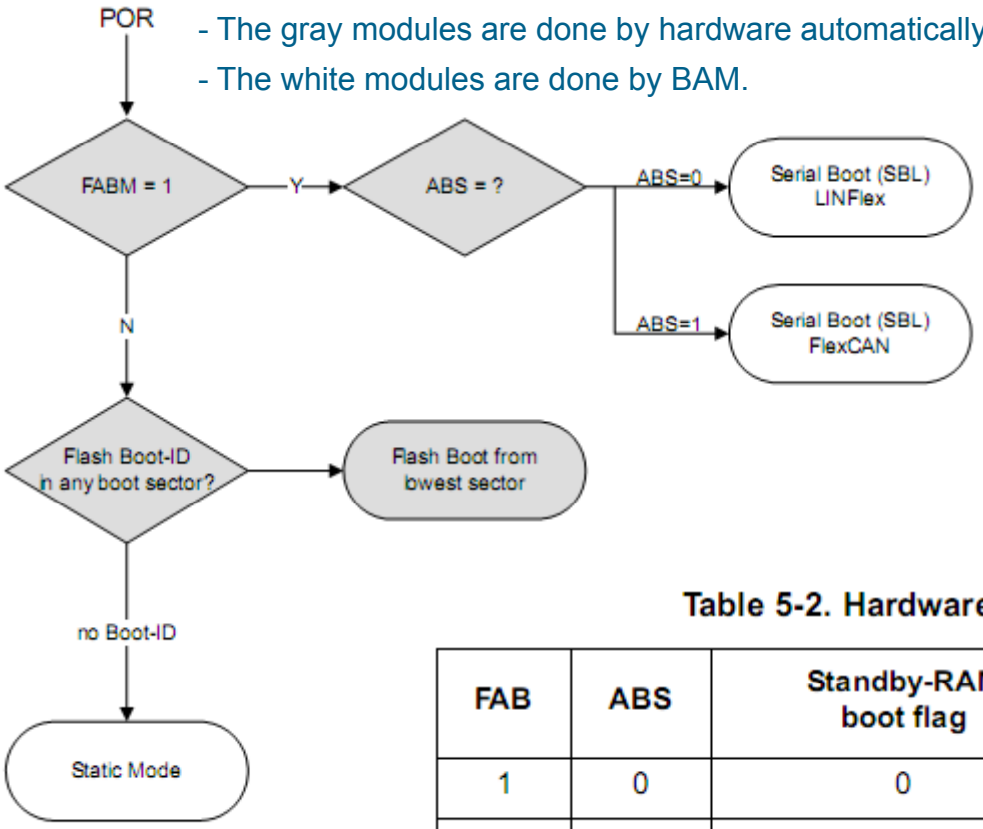

Figure 5-1.

❖Two boot modes are supported

-Single Chip: boot from the first bootable section of the Flash main array.

- Serial Boot: download boot code from either LINFlex or FlexCAN interface and then execute it.

Table 5-2. Hardware configuration to select boot mode

FAB	ABS	Standby-RAM boot flag	Boot ID	Boot mode
1	0	0	—	LINFlex
1	1	0	—	FlexCAN
0	—	0	Valid	SC (Single Chip)
0	—	0	Not found	Static mode

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Boot from Single Chip Mode

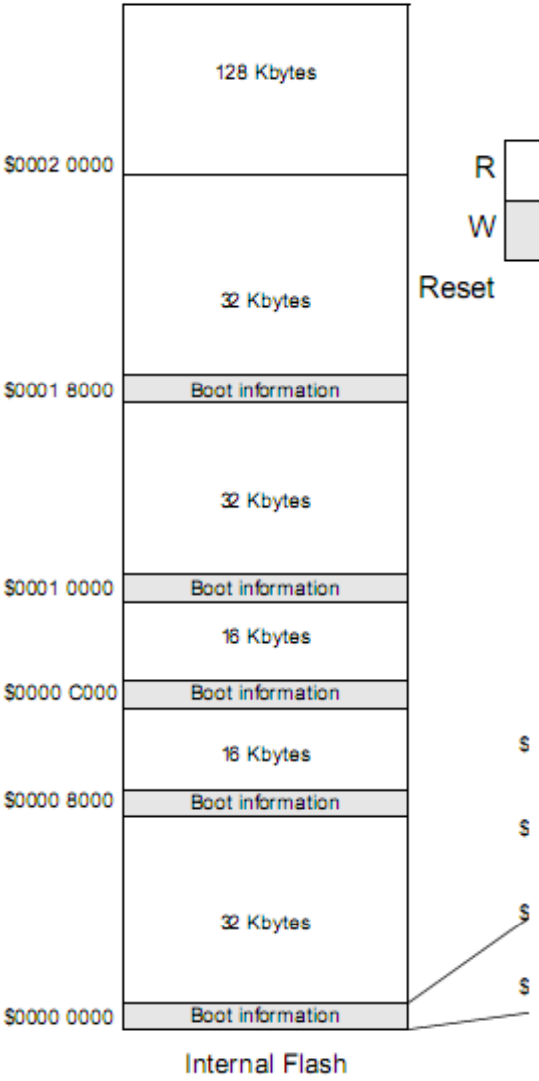

Figure 5-2. Reset Configuration Half Word (RCHW)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	Reserved								BOOT_ID[0:7]							
W																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- MPC560xB Flash is partitioned into boot sectors as shown in the left diagram. Each boot sector contains at offset 0x00 the Reset Configuration Half-Word (RCHW)
- In single chip boot mode the hardware searches a flash boot sector for a valid boot ID. As soon the device detects a bootable sector, it jumps within this sector and reads the 32-bit word at offset 0x4. The word is the address where the startup code is located.
- If a valid RCHW is not found, the BAM code is executed, in this case, BAM just put MPC560xB into static mode (low power SAFE mode).

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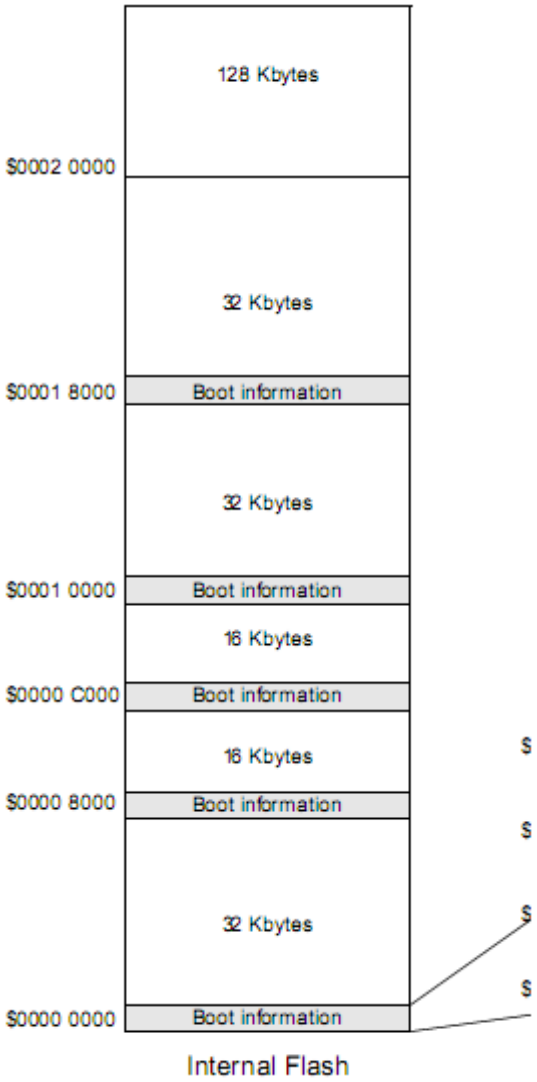
BAM Overview



- BAM is only executed in either one of the following two cases:
  - Serial boot mode is selected by FAB pin
  - Hardware has not found any valid ID in boot sectors.
  - If one of above case is true, the device fetches code at address 0xffff_c000 and execute the BAM software.

Table 5-1. BAM memory organization

Parameter	Address
BAM entry point	0xFFFF_C000
Downloaded code base address	0x4000_0100

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BAM Logic Flow

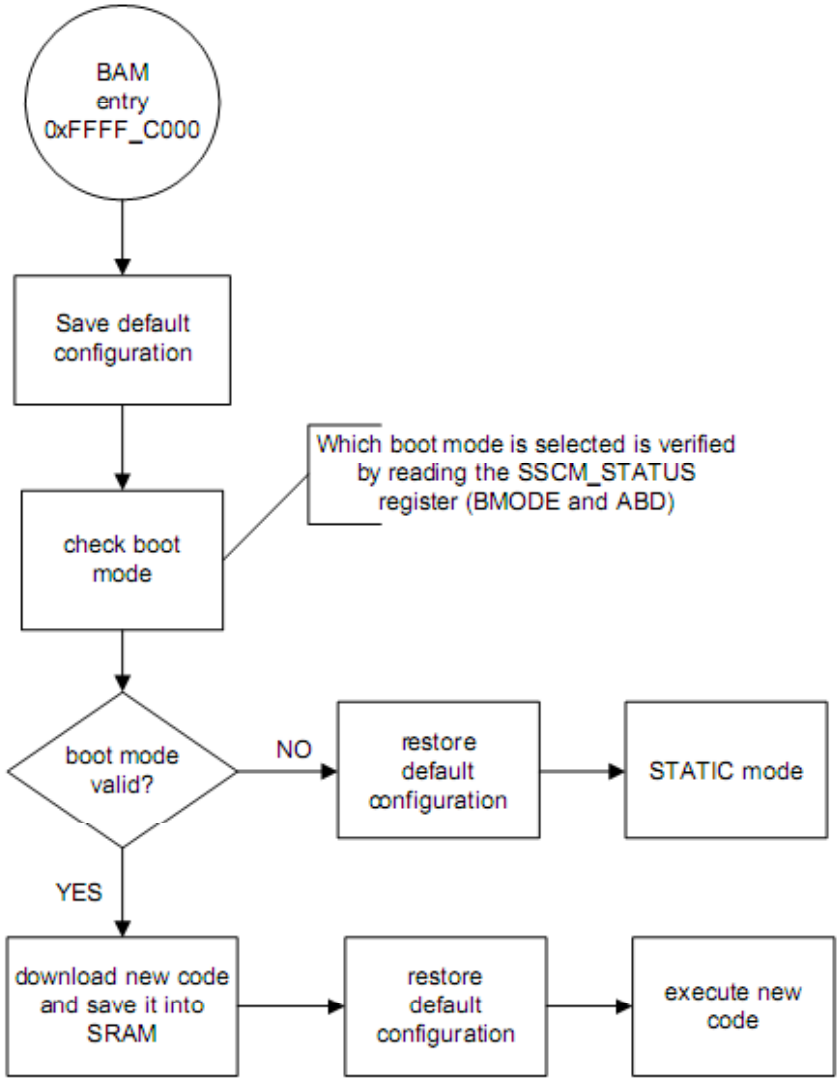

Figure 5-4. BAM logic flow

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From a high level perspective, the download protocol follows these steps:

1. Send 64-bit password
2. Send start address, size of downloaded code in bytes and VLE bit[1]
3. Download data
4. Execute code from start address

Each step must be completed before the next step starts.

The communication is done in half duplex manner, any transmission from the host is followed by the MCU transmission:

- Host sends data to MCU and starts waiting
- MCU echoes to host the data received
- Host verifies if echoes is correct
  - If data is correct host can continue to send data
  - If data is not correct host stops to transmit and MCU need to be reset

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Table 5-7. UART boot mode download protocol

Protocol step	Host sent message	BAM response message	Action
1	64-bit password (MSB first)	64-bit password	Password checked for validity and compared against stored password.
2	32-bit store address	32-bit store address	Load address is stored for future use.
3	VLE bit + 31-bit number of bytes (MSB first)	VLE bit + 31-bit number of bytes (MSB first)	Size of download are stored for future use. Verify if VLE bit is set to 1
4	8 bits of raw binary data	8 bits of raw binary data	8-bit data are packed into a 32-bit word. This word is saved into SRAM starting from the "Load address". "Load address" increments until the number of data received and stored matches the size as specified in the previous step.
5	None	None	Branch to downloaded code

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Boot from FlexCAN

Table 5-8. FlexCAN boot mode download protocol

Protocol step	Host sent message	BAM response message	Action
1	CAN ID 0x011 + 64-bit password	CAN ID 0x001 + 64-bit password	Password checked for validity and compared against stored password
2	CAN ID 0x012 + 32-bit store address + VLE bit + 31-bit number of bytes	CAN ID 0x002 + 32-bit store address + VLE bit + 31-bit number of bytes	Load address is stored for future use. Size of download are stored for future use. Verify if VLE bit is set to 1
3	CAN ID 0x013 + 8 to 64 bits of raw binary data	CAN ID 0x003 + 8 to 64 bits of raw binary data	8-bit data are packed into 32-bit words. These words are saved into SRAM starting from the "Load address". "Load address" increments until the number of data received and stored matches the size as specified in the previous step.
5	None	None	Branch to downloaded code

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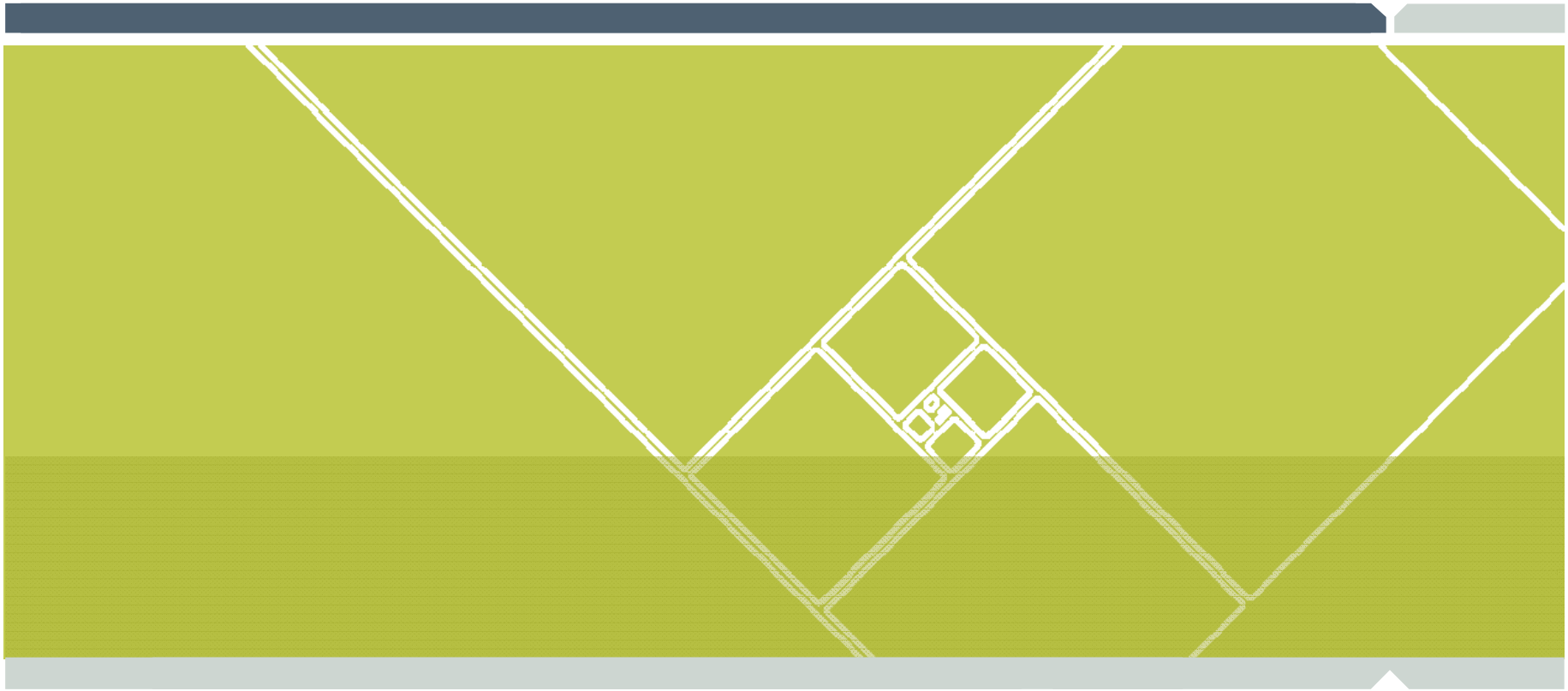
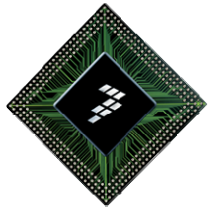


9. ADC/CTU/EMIOS



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ADC

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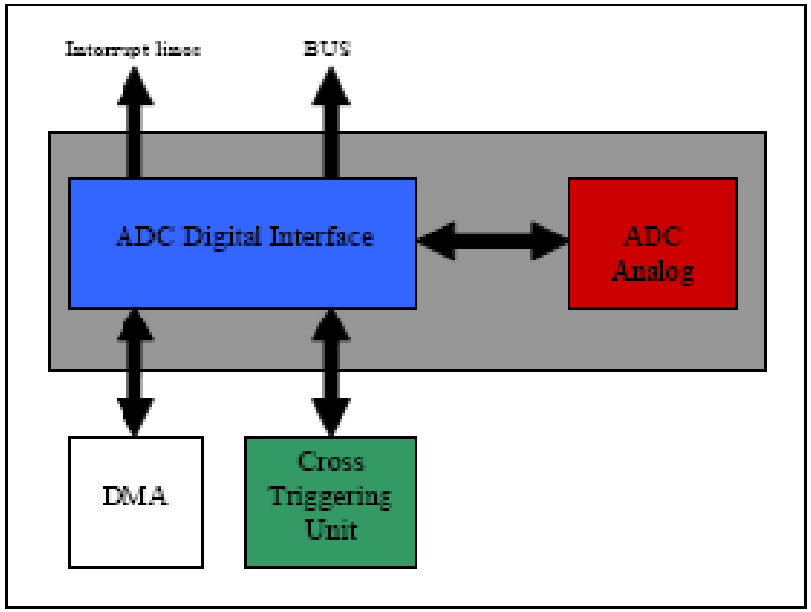
ADC overview



10-bit ADC resolution, on MPC5605/6/7B additional 12 Bit ADC

- Supports conversions time down to 650ns
- internal clock will be system clock/2
- ADC is specified from 6MHz to 32MHz
- Up to 36 single ended inputs channels, expandable to 64 channels with external multiplexers
- Internally multiplexed channels
  - 10-bit ± 2 counts accuracy (TUE) available for 16ch
  - 10-bit ± 3 counts accuracy (TUE) available for up to 20ch
- Externally multiplexed channels

— 10-bit ± 3 counts accuracy (TUE) available for up to 32ch

— Internal control to support generation of external analog multiplexer selection

- Dedicated result register available for every internally and externally muxed channel
- 3 independently configurable sample and conversion times for high occurrence channels, internally muxed channels and externally muxed channels
- Support for one-shot, scan, injection and triggered injected (CTU) conversion modes
- Independently configurable parameters for channels

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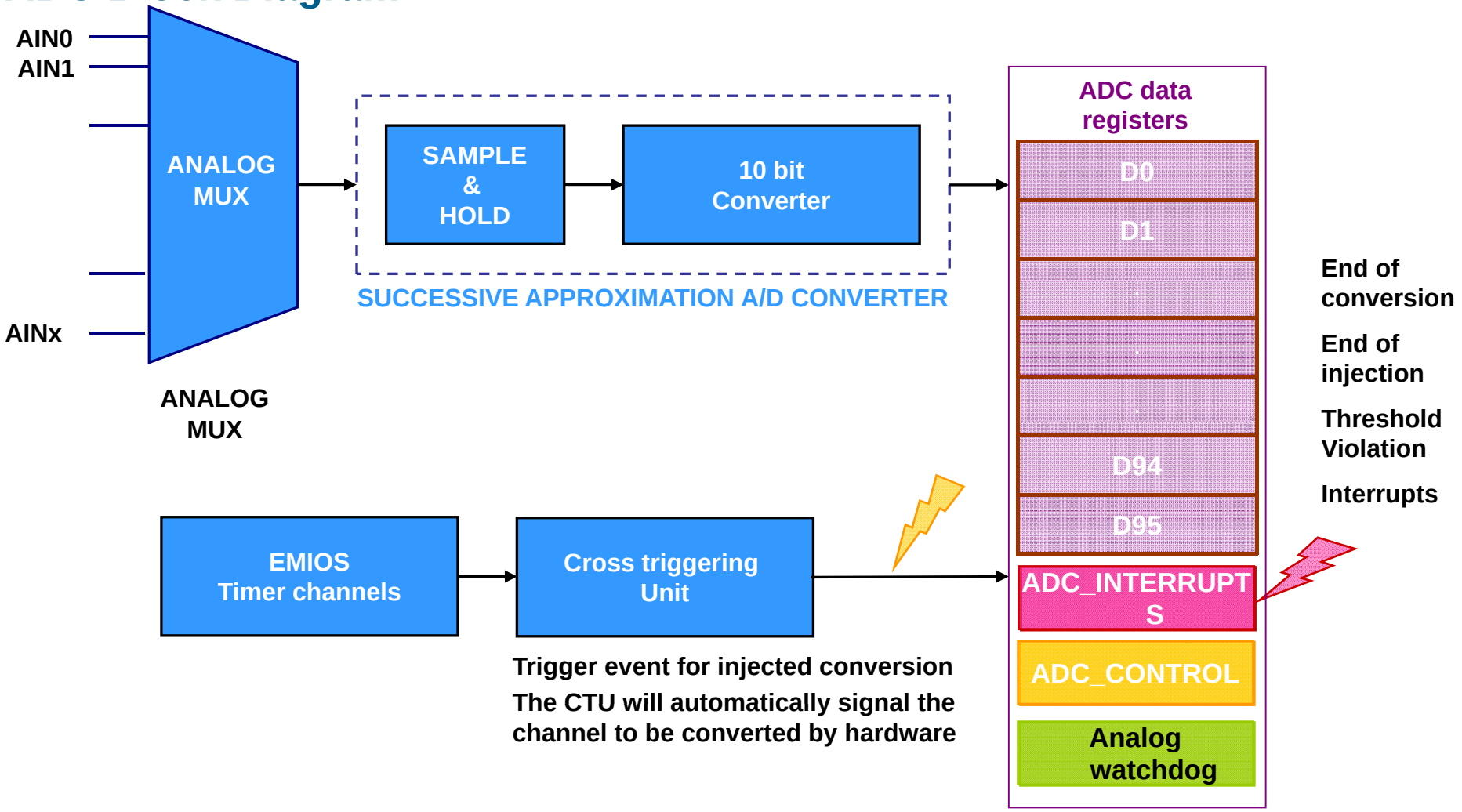
ADC Block Diagram



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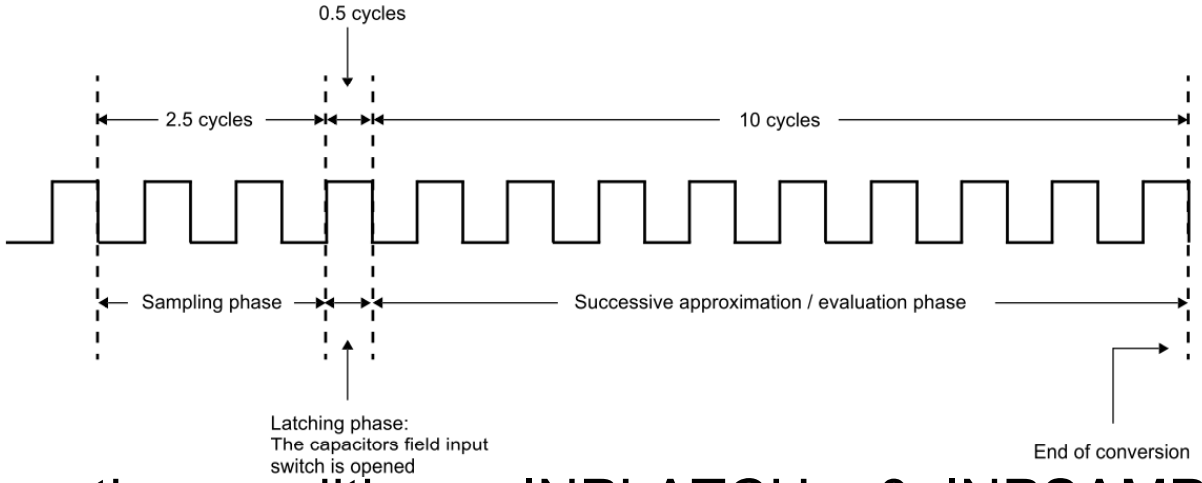
ADC Sampling and Conversion Timings

Sampling and conversion sequence:



Example: Operating conditions - INPLATCH = 0, INPSAMP = 3, INPCMP = 1 and F_{adc_clk} = 20 MHz

$T_{sample} = (INPSAMP – ndelay) . T_{ck}$

- INPSAMP ≥ 3, ndelay = 0.5 if INPSAMP ≤ 06h, otherwise = 1

$T_{eval} = 10 . (INPCMP . T_{ck})$

- INPCMP ≥ 1 and INPLATCH < INPCMP

$T_{conv} = T_{sample} + T_{eval} + (ndelay . T_{ck})$

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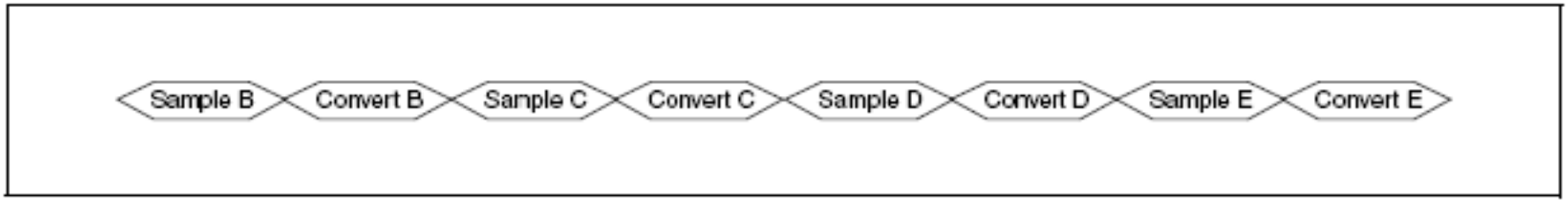
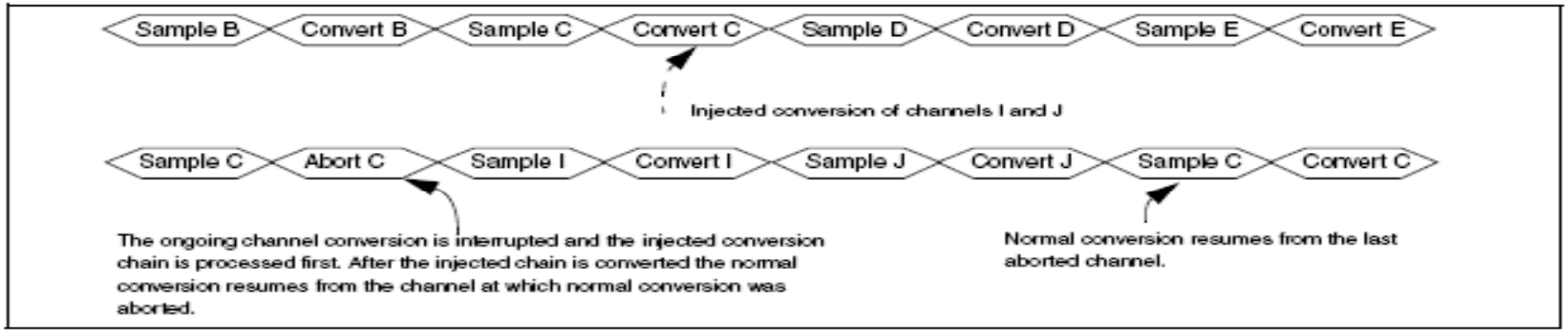
Normal conversion mode

one–shot mode or scan mode possible



Injected conversion mode


Sample B
Convert B
Sample C
Convert C
Sample D
Convert D
Sample E
Convert E
Injected conversion of channels I and J
Sample C
Abort C
Sample I
Convert I
Sample J
Convert J
Sample C
Convert C
The ongoing channel conversion is interrupted and the injected conversion chain is processed first. After the injected chain is converted the normal conversion resumes from the channel at which normal conversion was aborted.
Normal conversion resumes from the last aborted channel.

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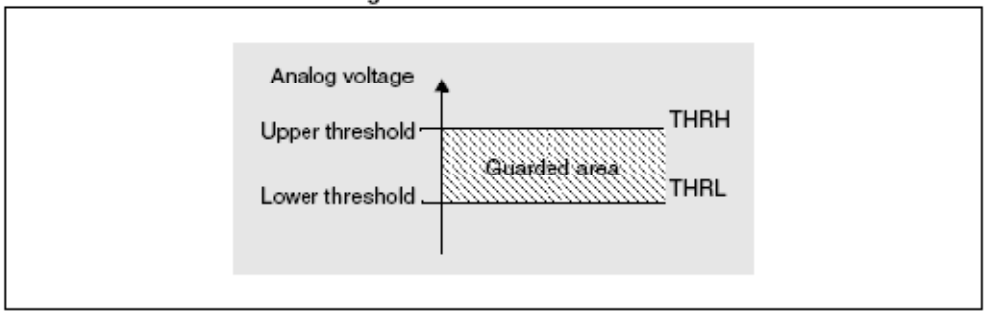
ADC analog watchdogs

- The ADC supports 4 analog watchdogs with
  - Interrupt capability
  - Allow continuous hardware monitoring of 4 analog input channels

The analog watchdogs are used for determining whether the result of a channel conversion lies within a given guarded area specified by an upper and a lower threshold value named THRH and THRL respectively.

Figure 25-6. Guarded area



After the conversion of the selected channel, a comparison is performed between the converted value and the threshold values. If the converted value lies outside that guarded area then corresponding threshold violation interrupts are generated.

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I/O Module

eMIOS

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eMIOS

BOLERO family offers up to two eMIOS modules (0 and 1) with 28 channels each. Each eMIOS features input capture, output compare, PWM and GPIO modes *(Not all modes on all channels)*

5 x 16-bit counter busses (independent time bases)

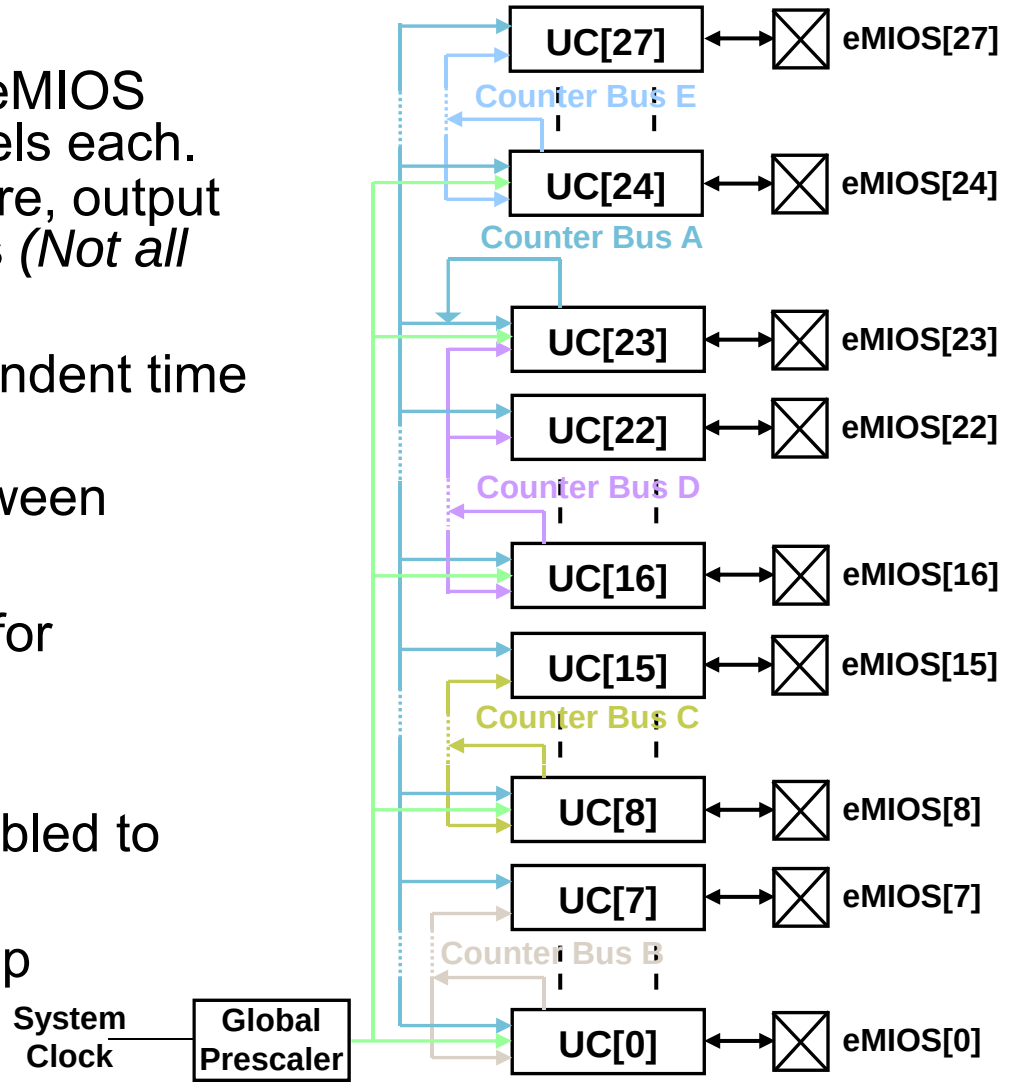
A counter bus can be shared between different channels

Programmable clock prescalers (for channels 0, 8, 16, 23 & 24)

Programmable input filter

Channels can be individually disabled to assist with power saving

The two eMIOS modules start/stop synchronously



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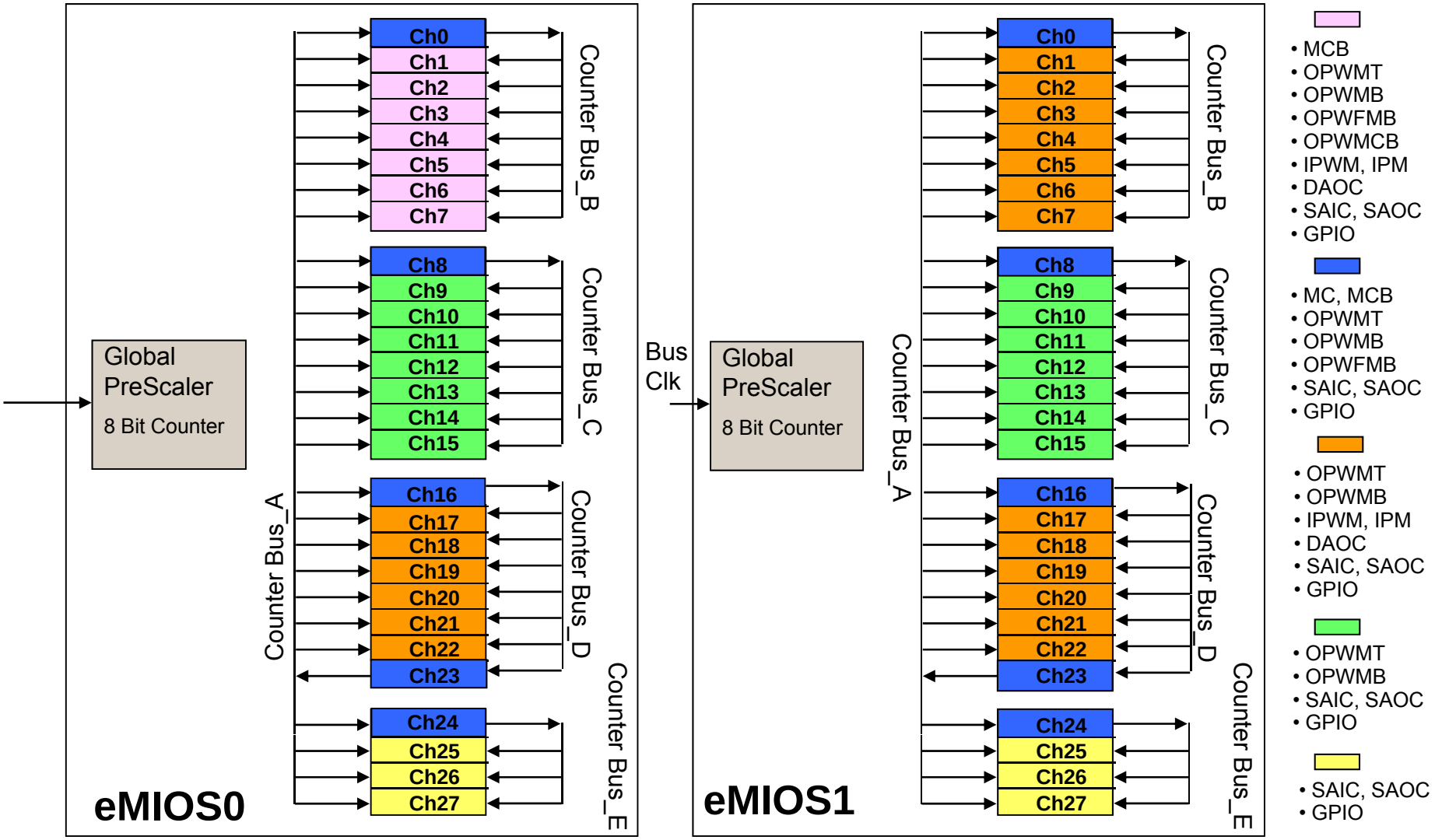
eMIOS Channel Configuration



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eMIOS Channel Type

Description	Name	Channel Type				
		Type X	Type Y	Type F	Type G	Type H
General Purpose Input / Output	GPIO	x	x	x	x	x
Single Action Input Capture	SAIC	x	x	x	x	x
Single Action Output Compare	SAOC	x	x	x	x	x
Modulus Counter	MC	x	-	-	-	-
Modulus Counter Buffered (Up / Down)	MCB	x	-	-	x	-
Input Pulse Width Measurement	IPWM	-	-	-	x	x
Input Period Measurement	IPM	-	-	-	x	x
Double Action Output Compare	DAOC	-	-	-	x	x
Output Pulse Width and Frequency Modulation Buffered	OPWFMB	x	-	-	x	-
Center aligned Output PWM Buffered with dead time	OPWMCB	-	-	-	x	-
Output Pulse Width Modulation Buffered	OPWMB	x	x	-	x	x
Output Pulse Width Modulation Trigger	OPWMT	x	x	-	x	x

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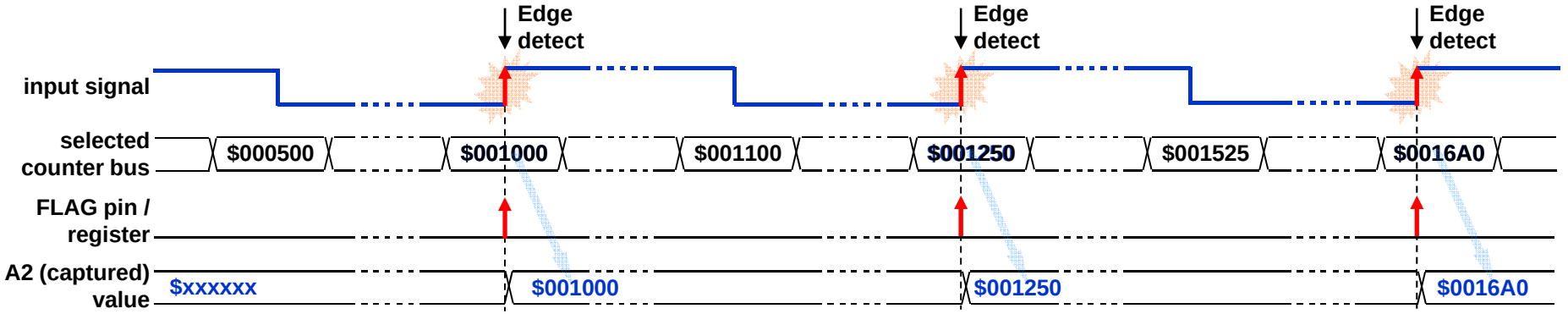
eMIOS Modes
Single Action Input Capture

Returns the **value** of the counter bus on an edge match of an input signal .

- Can use Internal or Modulus counter
- Can match on Rising, Falling or Toggle determined by state of EDPOL, EDSEL



Notes: (Example with detection on rising edge)

- When edge is detected, flag is set and counter bus value is captured in register A2. User reads this value from UCA[n] register.
- UCB[n] = Cleared and cannot be written

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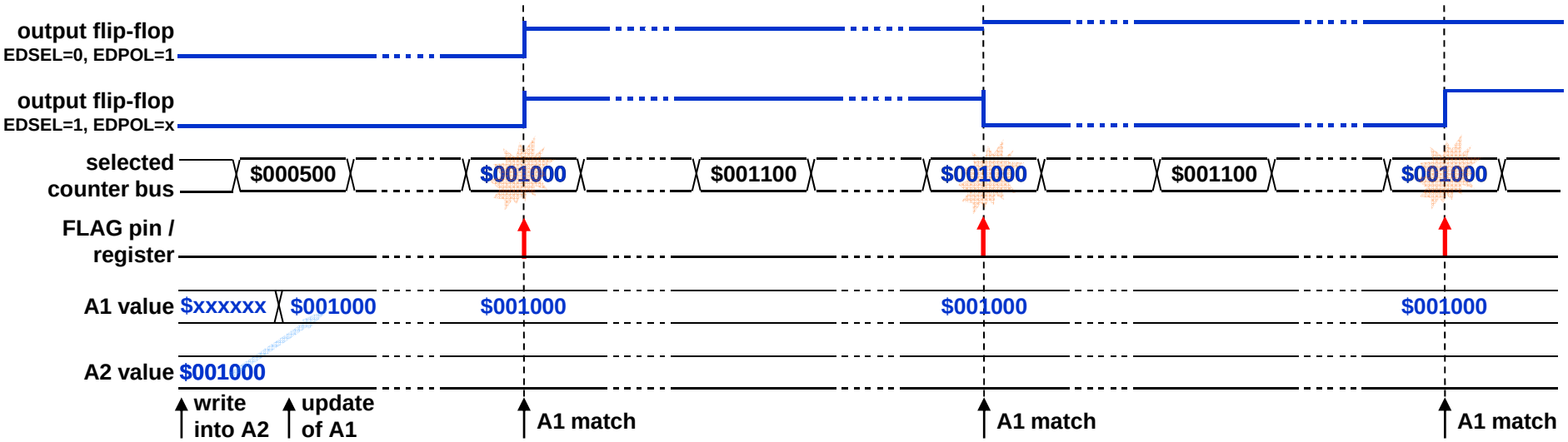
Generates an output on a counter bus match

- Can use Internal or Modulus counter
- Can set output to go HIGH, LOW or TOGGLE, based on the state of EDPOL and EDSEL



Notes:

- Write the desired counter bus value to create a match into UCA[n] (A2n) which is buffered into A1.
- A comparator match of A1 results in an output event, defined by status of EDPOL and EDSEL

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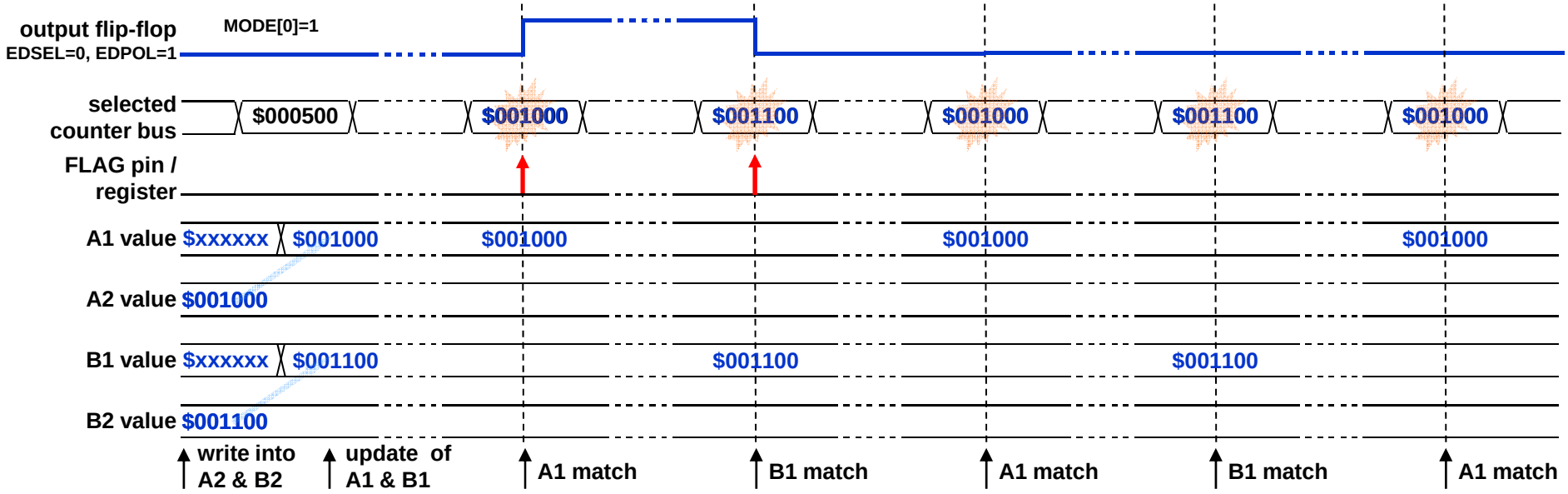
eMIOS Modes
Double Action Output Compare

Generates an output pulse

- Can use Internal or Modulus counter
- Polarity of pulse is determined by value of EDPOL



Notes:

- Write the desired pulse leading edge into UCA[n] (A2n) and the falling edge into UCB[n] (B2n) which are buffered into A1 and B1.
- On a comparator A match, the output is set to the value of EDPOL. FLAG is set if MODE0=1
- On a comparator B match, the output is set to the inverse of EDPOL. FLAG is set

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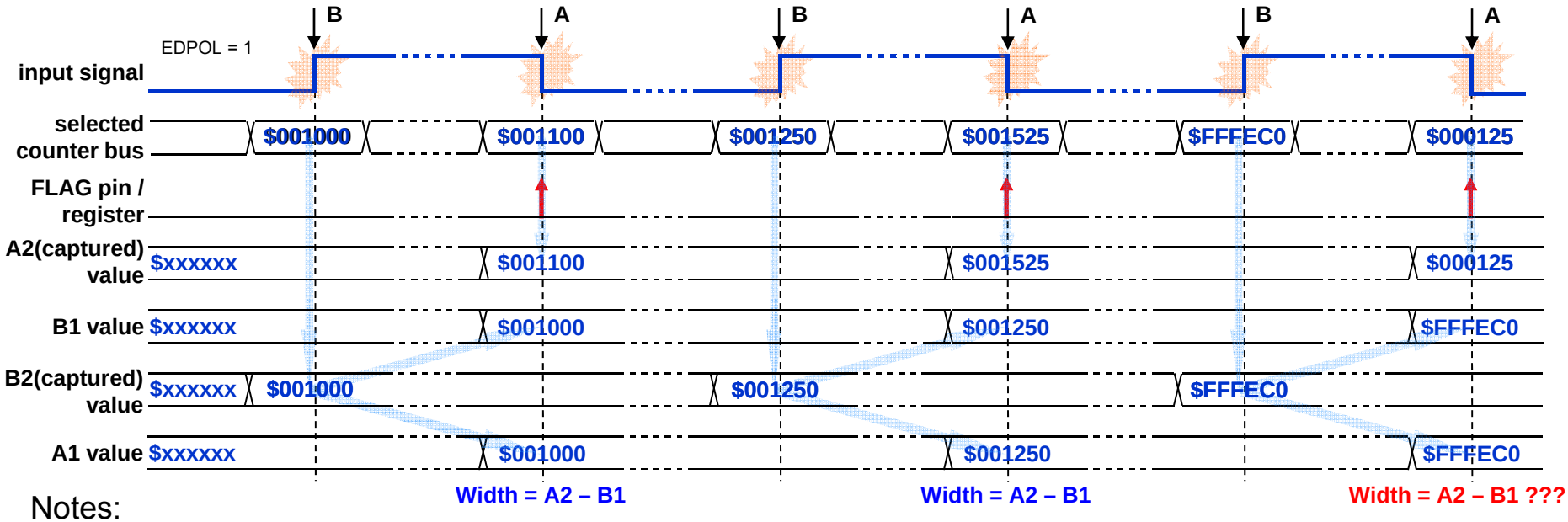
Input Pulse Width Measurement

Determines the **width** (in counter bus clock ticks) of an input pulse width

- Can use Internal or Modulus counter
- Can be configured to measure HIGH or LOW pulses by state of EDPOL bit (EDPOL=1 for HIGH)



Notes:

- Leading edge is captured into B2[n]. (EDPOL Determines if leading edge is high or low).
- Trailing edge is captured into A2[n] and Flag is set
- Pulse width is calculated by subtracting UCBn (B1) from UCAn (A2)
- Caution – If pulse has spanned a counter bus period, then need to take care to modify calculation….
  Width = (UCAn + Counter Bus Period) - UCBn

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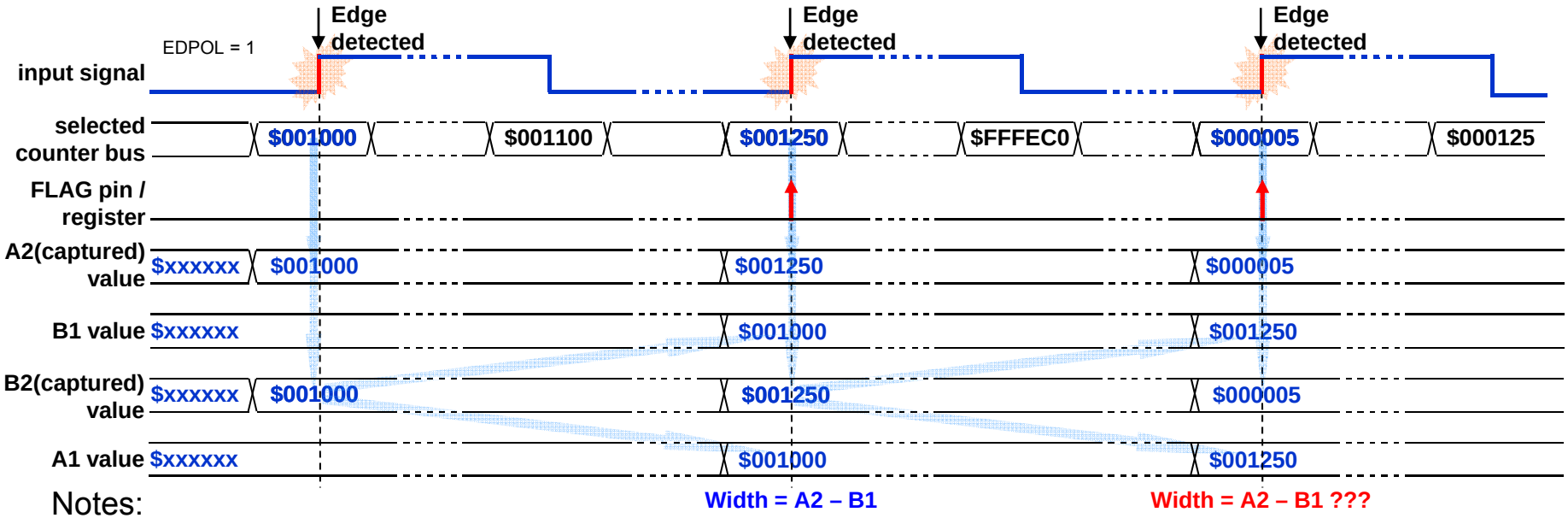
Input Period Measurement

Determines the **period** (in counter bus clock ticks) of an input pulse width

- Can use Internal or Modulus counter
- Can be configured to measure between 2 HIGH or 2 LOW edges, determined by the state of the EDPOL bit



Notes:

- When the edge of the selected polarity is detected, counter value is captured into A2[n] and B2[n], the data previously held in B2[n] is captured into A1[n] and B1[n], and Flag is set.
- Period is calculated by subtracting UCBn (B1) from UCAn (A2)
- Caution – If period of input signal has spanned a counter bus period, then need to take care to modify calculation…. Width = (UCAn + Counter Bus Period) - UCBn

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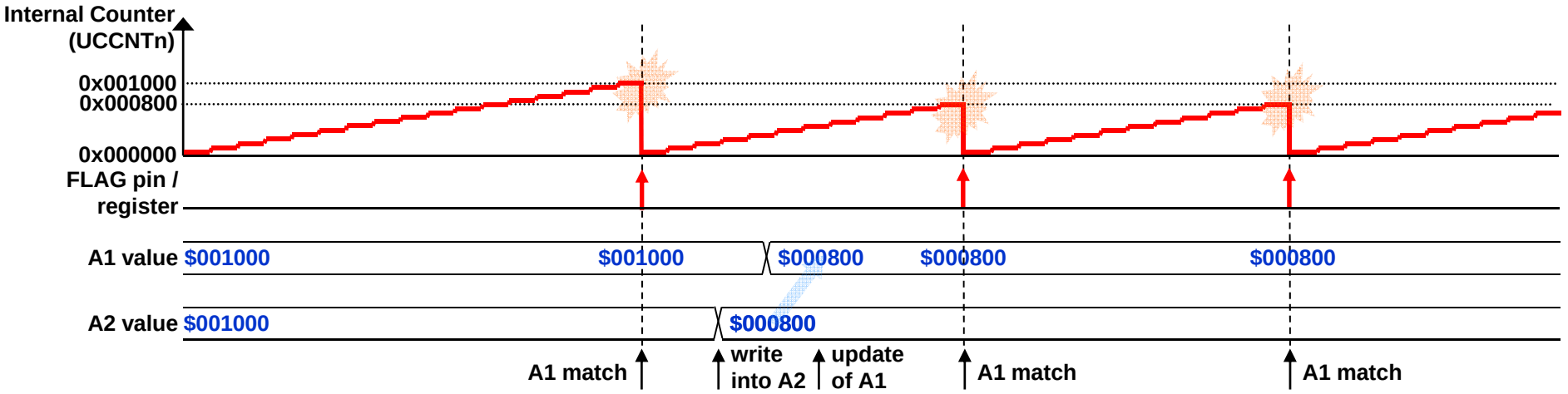
Generates a time base which can be shared with other channels through the internal counter bases

- Can use Internal or External (input channel pin) counter



Notes:

- On a comparator A match, FLAG is set and the internal counter is set to value $0.
- A change of the A2 register makes the A1 register be updated at the next clock.
- Caution – If when entering MC mode the internal counter value is upper than register UCA[n] value, then it will wrap at the maximum counter value ($FFFFFF) before matching A1.

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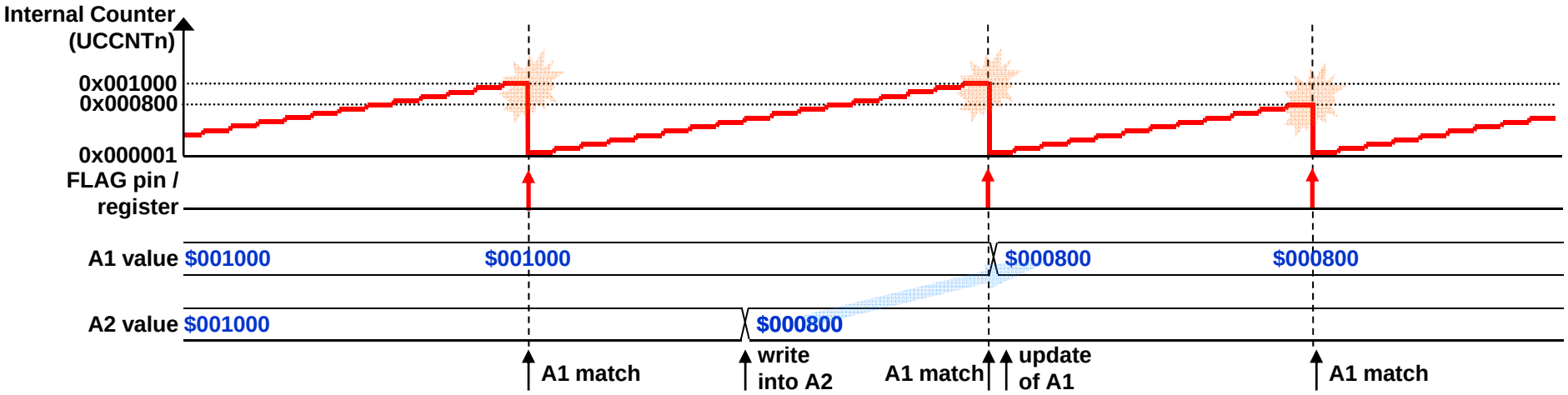

Notes:

- On a comparator A match, FLAG is set and the internal counter is set to value $1.
- Allowing smooth transitions, a change of the A2 register makes the A1 register be updated when the internal counter reaches the value $1.
- Caution – If when entering MCB mode the internal counter value is upper than register UCA[n] value, then it will wrap at the maximum counter value ($FFFFFF) before matching A1.

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Generates a time base which can be shared with other channels through the internal counter bases

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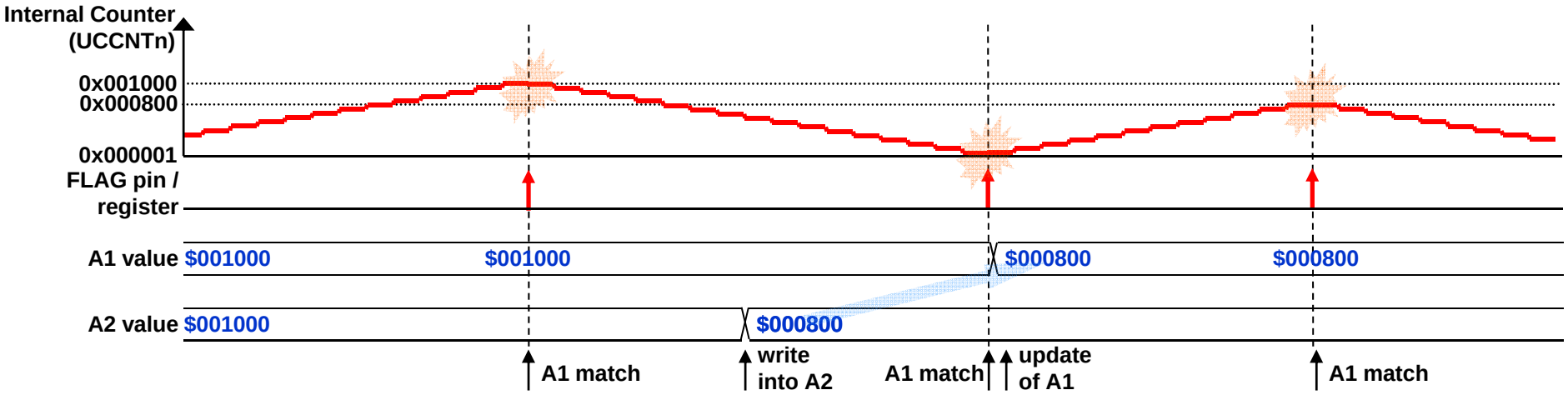

Notes:

- On a comparator A match, FLAG is set and the internal counter is set to value $1.
- Allowing smooth transitions, a change of the A2 register makes the A1 register be updated when the internal counter reaches the value $1.
- Caution – If when entering MCB mode the internal counter value is upper than register UCA[n] value, then it will wrap at the maximum counter value ($FFFFFF) before matching A1.

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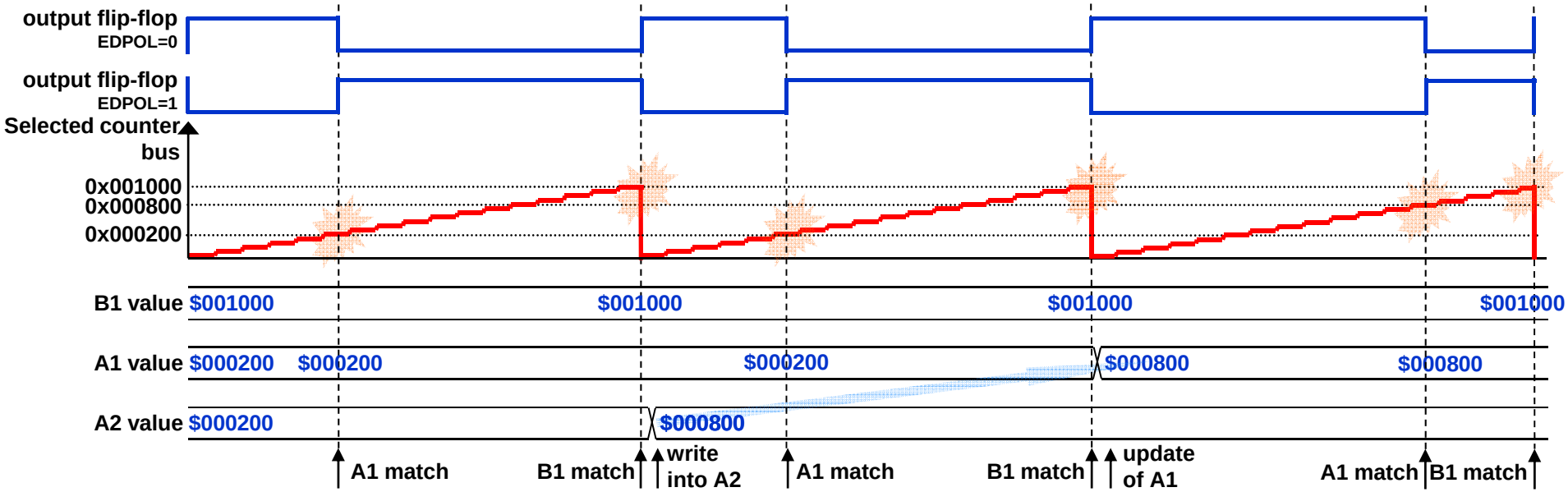
Generates a simple output PWM signal

- Requires **INTERNAL** Counter
- EDPOL allows selection between active HIGH or active LOW duty cycle.



Notes:

- Duty Cycle = UCA[n] (A1) + 1, Period = UCB[n] (B1) + 1
- On Comparator A1 match, Output pin is set to value of EDPOL
- On Comparator B1 match, Output pin is set to complement of EDPOL and Internal counter is reset
- The transfers from register B2[n] to B1[n] and from register A2[n] to A1[n] are performed at the first clock of the next cycle.
- FLAGS can be generated only on B1 matches or on both A1 and B1 matches depending on MODE[5] bit.

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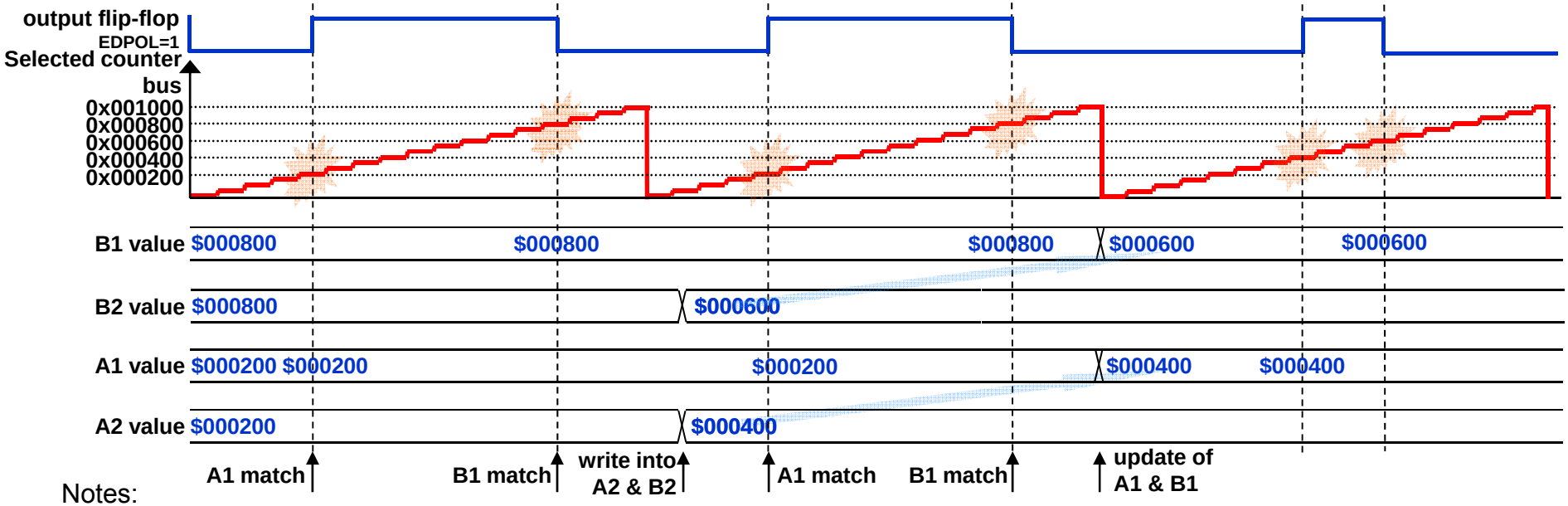
Generates a simple output PWM signal

- Can use Internal or Modulus counter
- EDPOL allows selection between active HIGH or active LOW duty cycle.



Notes:

- Write UCA[n] (A1) with Leading Edge. Write UCB[n] (B1) with trailing edge
- On Comparator A1 match, Output pin is set to value of EDPOL
- On Comparator B1 match, Output pin is set to complement of EDPOL
- The transfers from register B2[n] to B1[n] and from register A2[n] to A1[n] are performed at the first clock of the next cycle.
- FLAGS can be generated only on B1 matches or on both A1 and B1 matches depending on MODE[5] bit.

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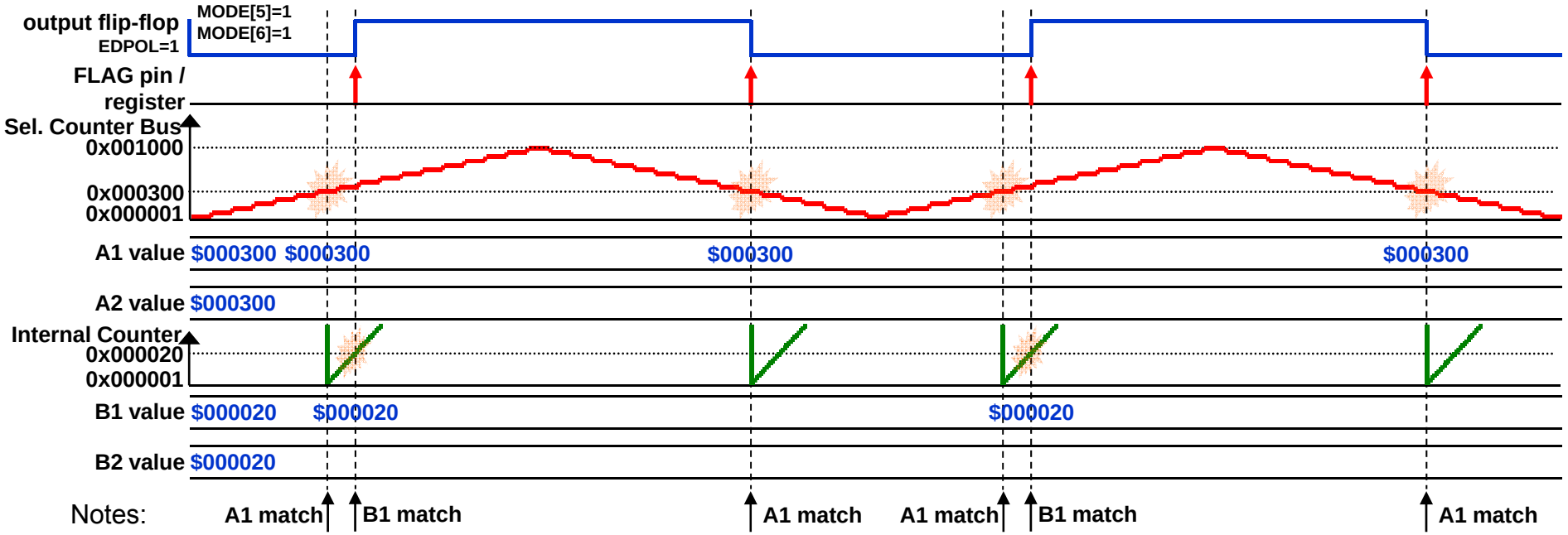
Generates a center aligned PWM output signal with dead time insertion

- MODE[6] bit selects between trailing and leading dead time insertion, respectively.
- EDPOL allows selection between active HIGH or active LOW duty cycle.
- Requires MCB UP/DOWN



Notes:

- Period = MCB Period, Dead Time = B1[n], Duty Cycle = 2 * (Period - A1[n]) – Dead Time
- On the selected dead time insertion edge:
  - On Comparator A1 match (Selected Counter Bus), the internal counter is set to $1
  - On Comparator B1 match (Internal Counter), Output pin is set to the value of EDPOL
- On the non-selected dead time insertion edge:
  - On Comparator A1 match, Output pin is set to complement of EDPOL and internal counter set to $1

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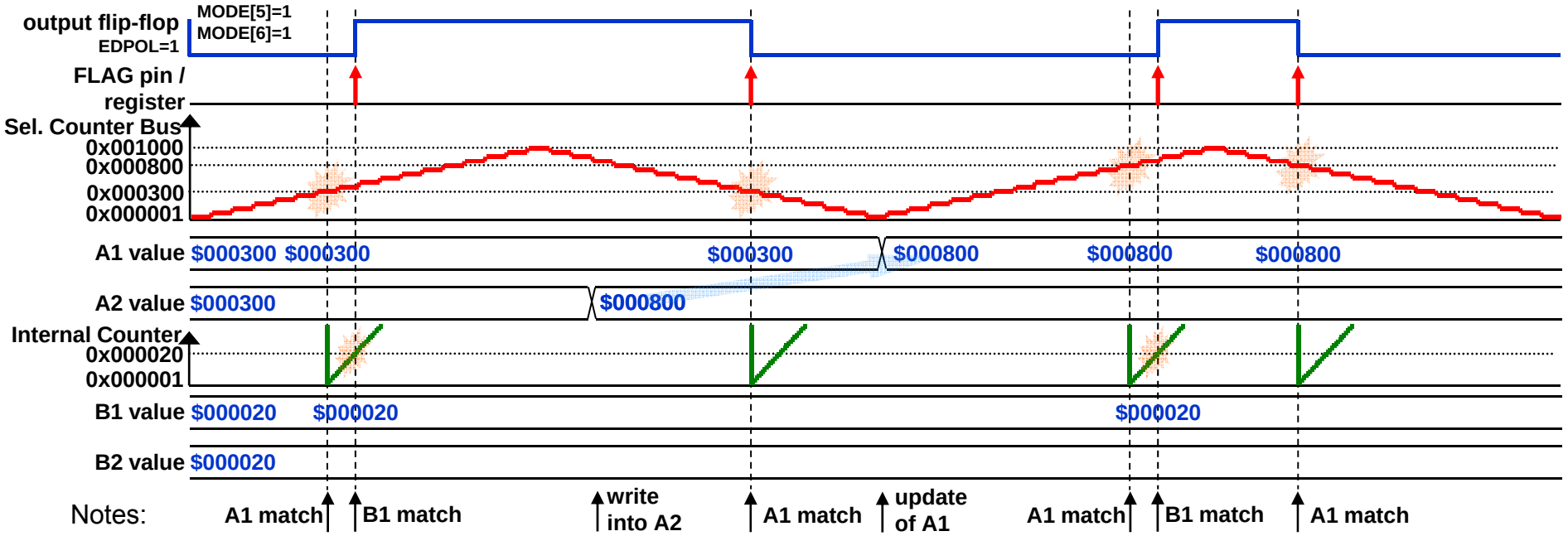

Notes:

- FLAGS can be generated only on B1 matches or on both A1 and B1 matches depending on MODE[5] bit.
- The transfers from register B2[n] to B1[n] and from register A2[n] to A1[n] are performed at the first clock of the next cycle.
- To achieve 100% duty cycle, A1[n] must be set to $1. To achieve 0% duty cycle, A1[n] must be set to a value greater than the maximum value of the selected time base.
- Caution – The internal counter should not reach $0 as consequence of a rollover.

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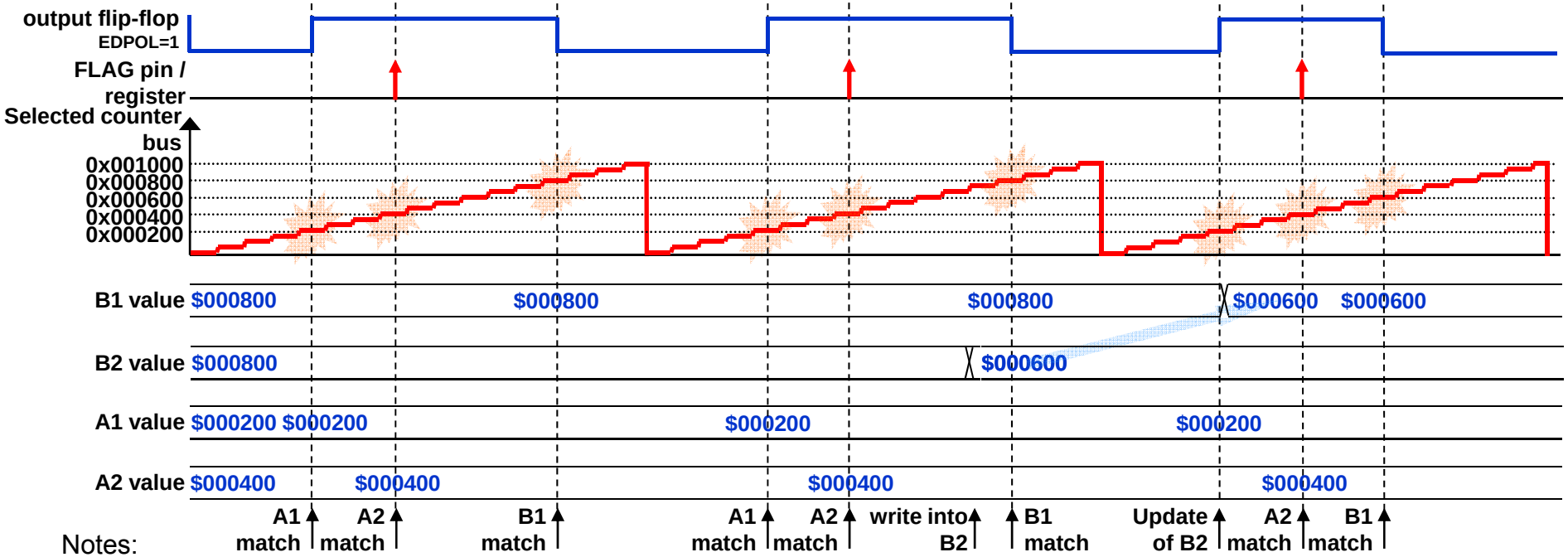
Generates a PWM signal with a fixed offset and a trigger signal

- Intended to be used with other channels in the same mode with shared common time base
- This mode is particularly useful in the generation of lighting PWM control signals.



Notes:

- A1[n] defines the Leading Edge, B1[n] the trailing edge, A2[n] the generation of a FLAG event
- On Comparator A1 match, Output pin is set to value of EDPOL
- On comparator A2 match, FLAG is set (and can allow to synchronize with other events, ie. AD conversion)
- On Comparator B1 match, Output pin is set to complement of EDPOL
- The transfers from register B2[n] to B1[n] is performed at every match of register A1

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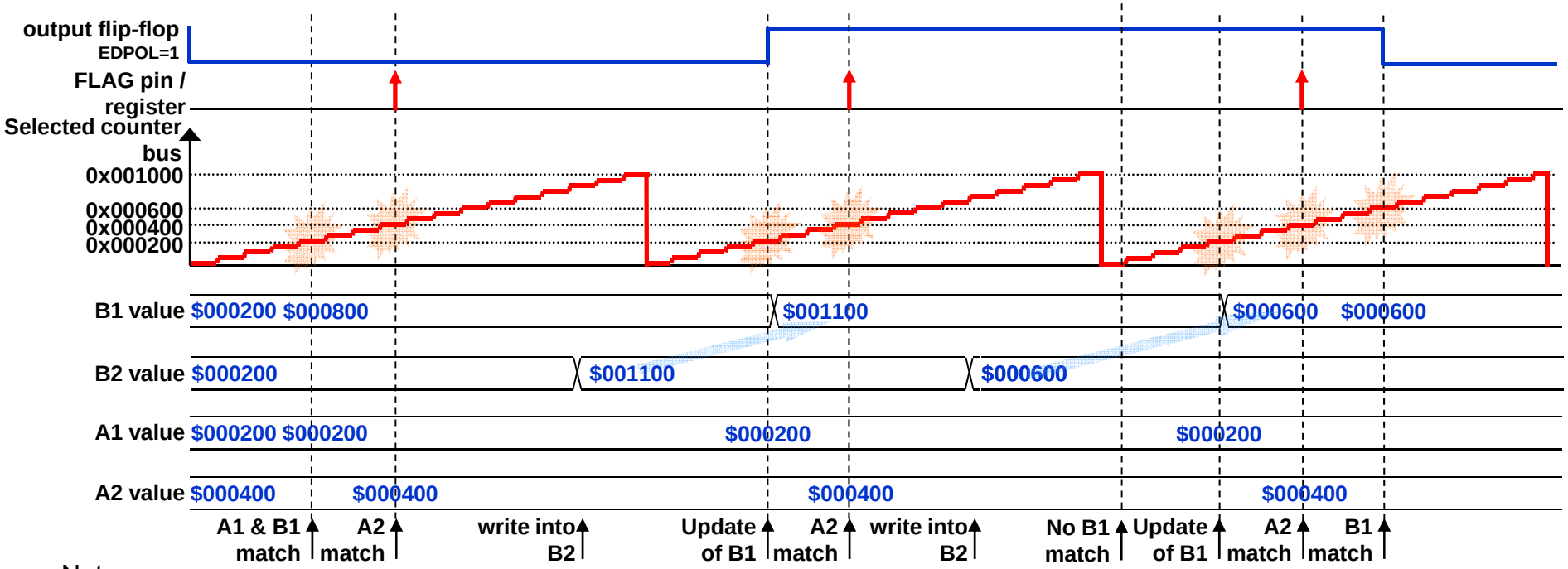

Notes:

- To achieve 0% duty cycle, both registers A1 and B1 must be set to the same value
- To achieve 100% duty cycle, the register B1 must be set to a value greater than the maximum value of the selected time base.

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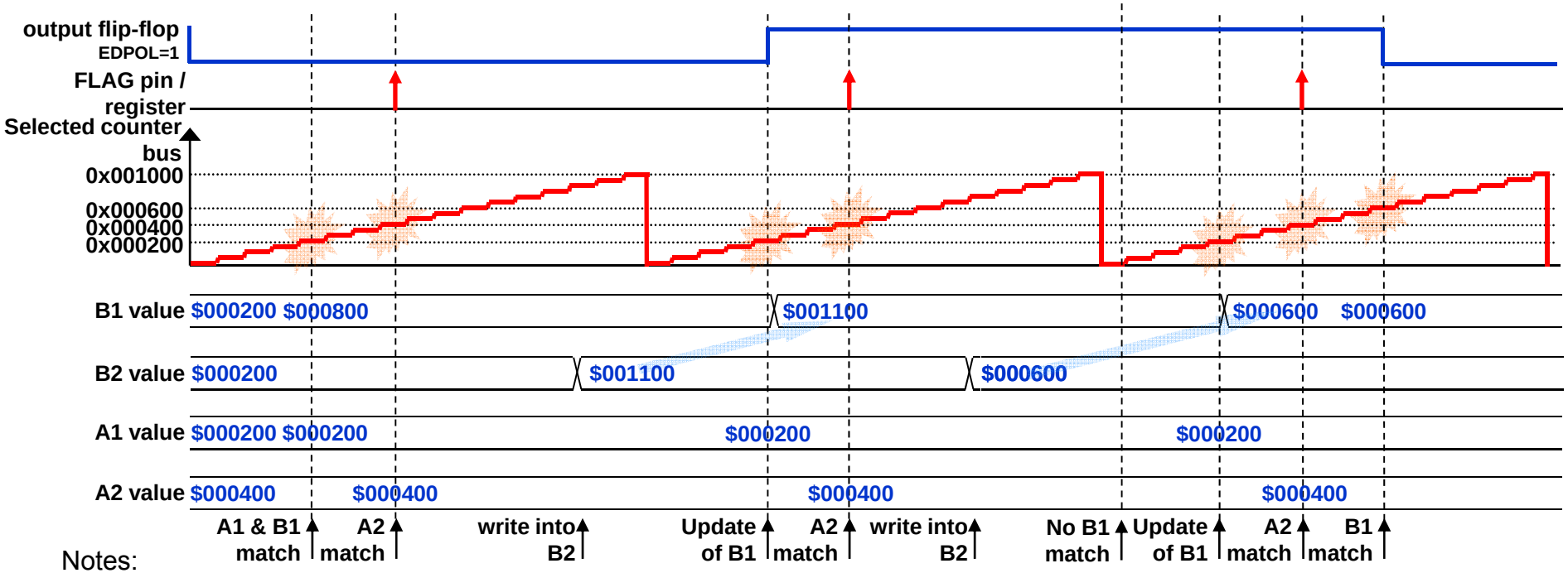

Notes:

- Caution – A2[n] value is not readable. A1[n] value is not writable and therefore cannot be configured in this mode (use GPIO mode for example).
- Caution – A2[n] is not buffered, its update is immediate
- Caution – Registers loaded with $0 will not produce matches if the time base is driven by a channel in MCB mode.

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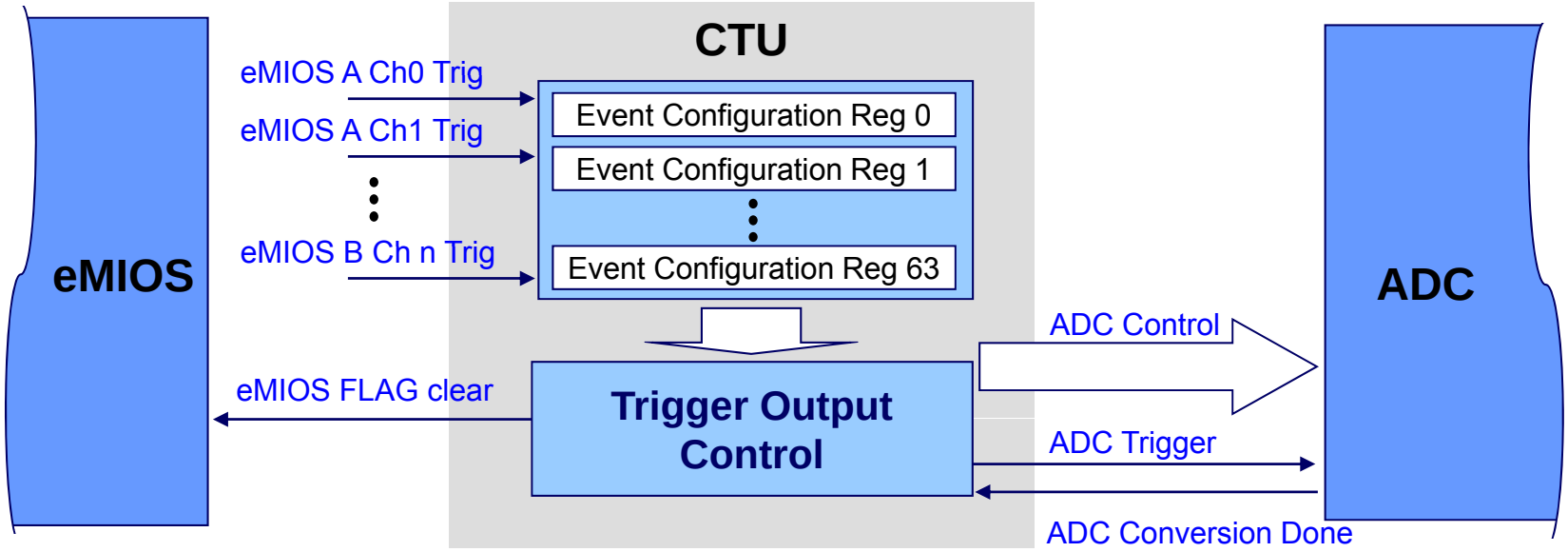
eMIOS/OPWMT
Trigger event

The trigger event generated by an OPWMT channel allows to synchronize ADC conversion w.r.t. PWM signal

The CTU (Cross Triggering Unit) can be configured to define the ADC channel to be converted on OPWMT channel trigger

Each ADC conversion result is stored in a dedicated result register (refer to ADC slides)



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CTU

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The Cross Triggering Unit Lite on the Bolero family is a link between timers (eMIOS or PIT) and the ADC

The CTU Lite automatically transforms timer events into ADC conversions without main CPU intervention

The real-time behavior (synchronization) between timer events and ADC conversions is guaranteed

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CTU features details:

- 64 timer events
- Each timer event can be assigned corresponding ADC channel
- Only one ADC conversion can be triggered at a time
- HW arbitration when simultaneous event occur
- Event priorities are HW defined
- Single cycle delayed trigger output. The trigger output is a combination of 64 (generic value) input flags/events connected to different timers in the system.
- Maskable interrupt generation whenever a trigger output is generated
- One event configuration register dedicated to each timer event allows to define the corresponding ADC channel
- Acknowledgment signal to eMIOS/PIT for clearing the flag
- Synchronization with ADC to avoid collision

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CTU Lite Block Diagram

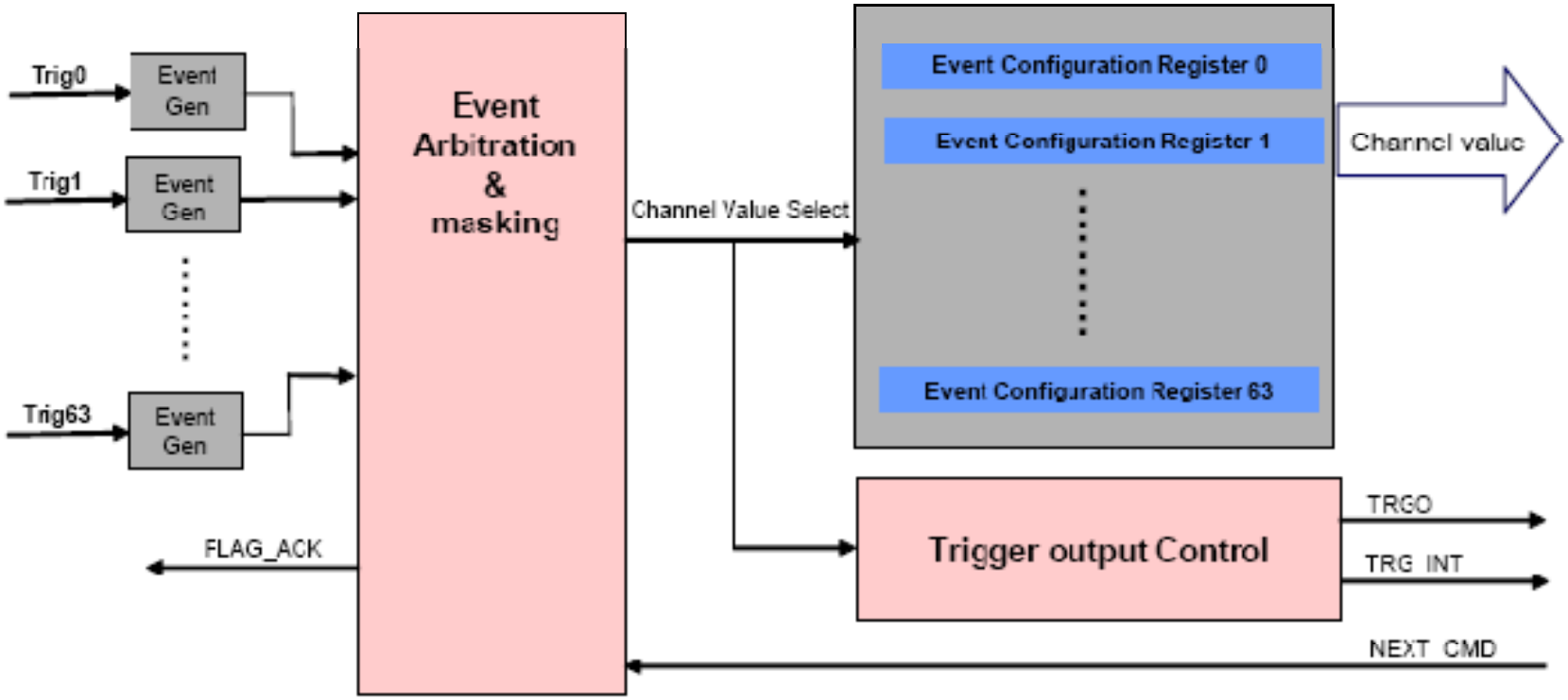

Figure 252. Cross Triggering Unit block diagram

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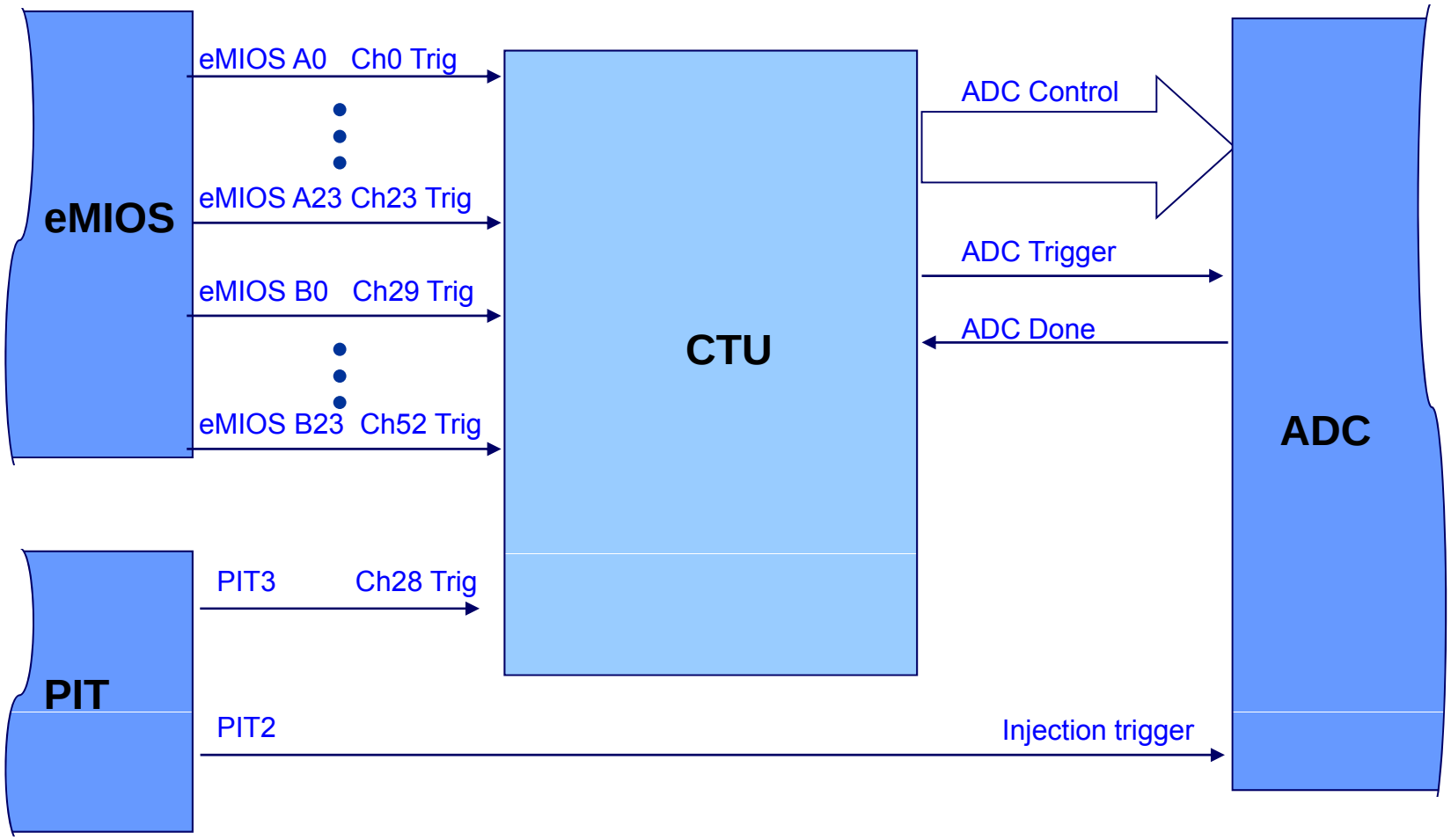
MPC5602/3/4B eMIOS260/OPWMT
Trigger event



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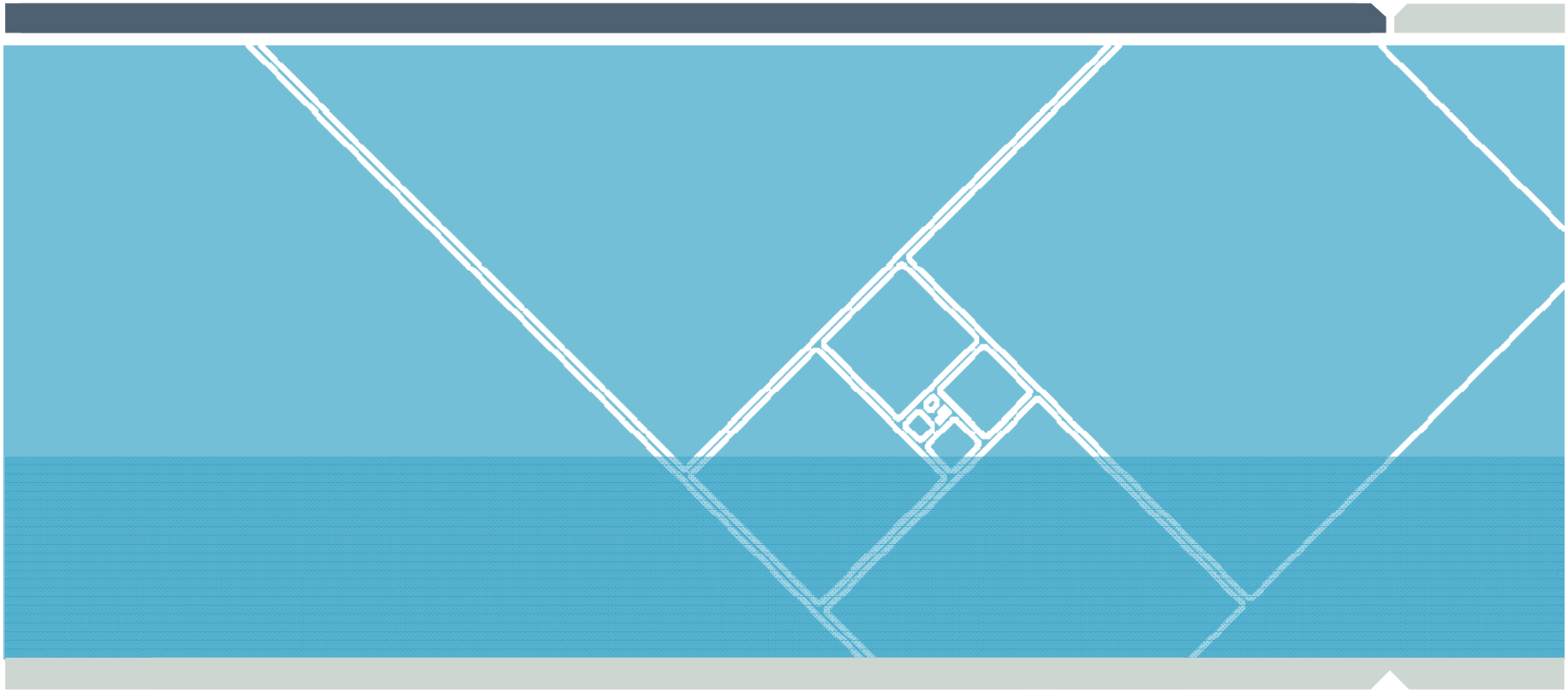

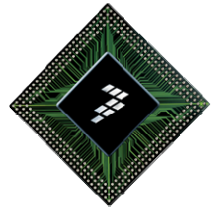

10. Hands-on Workshop

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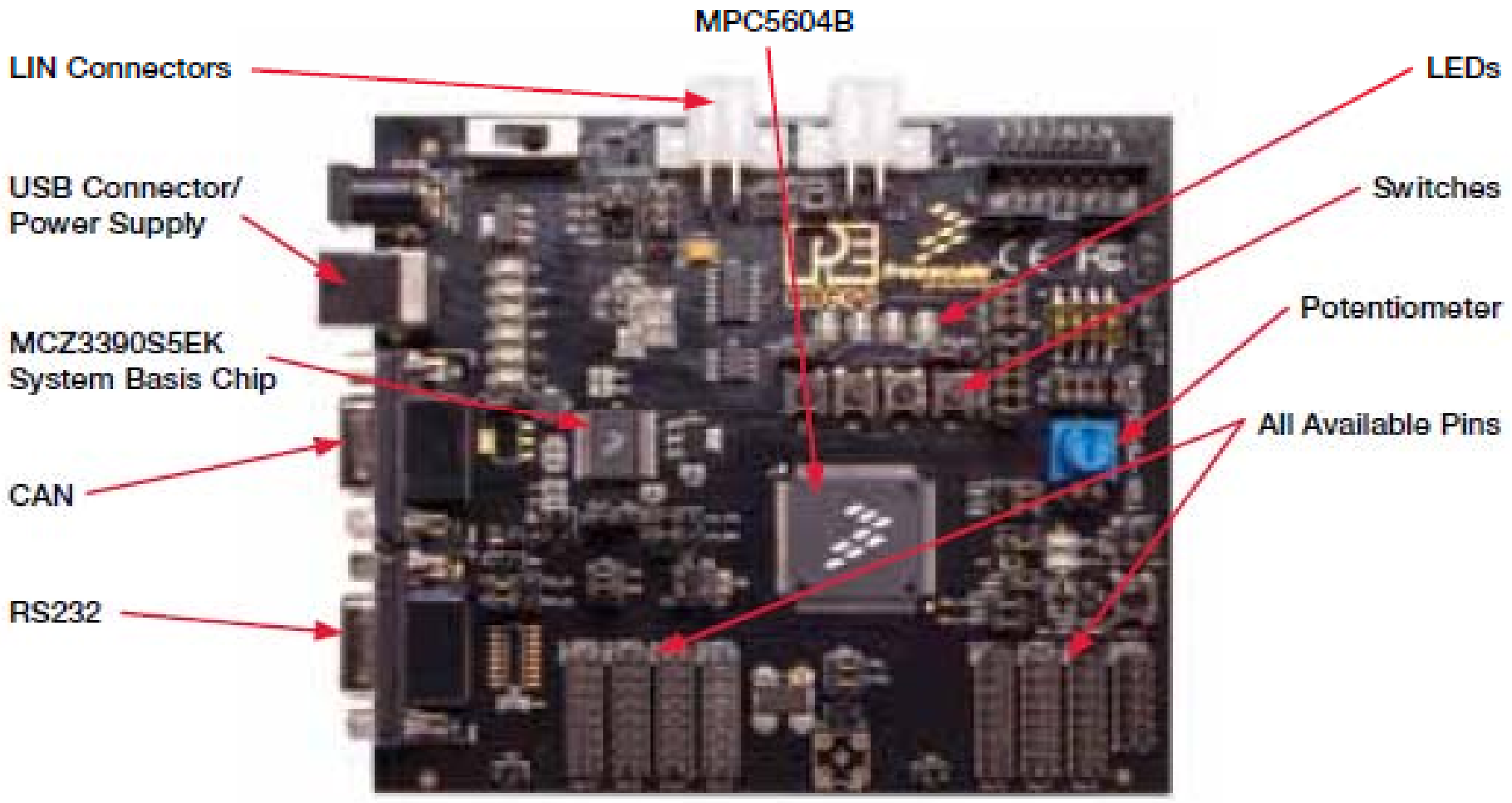
STARTER TRAK -- MPC5604B



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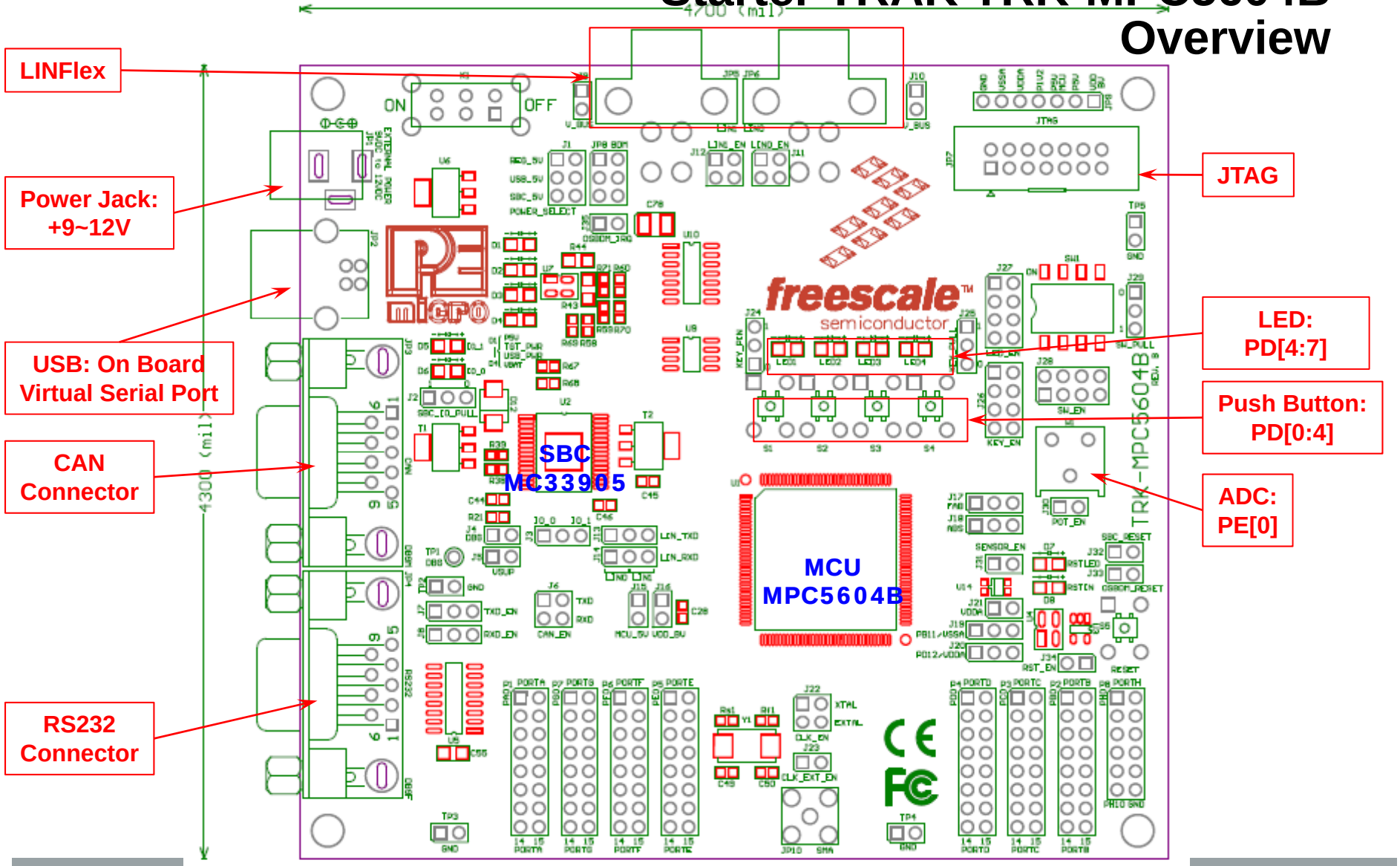
Starter TRAK TRK-MPC5604B Overview



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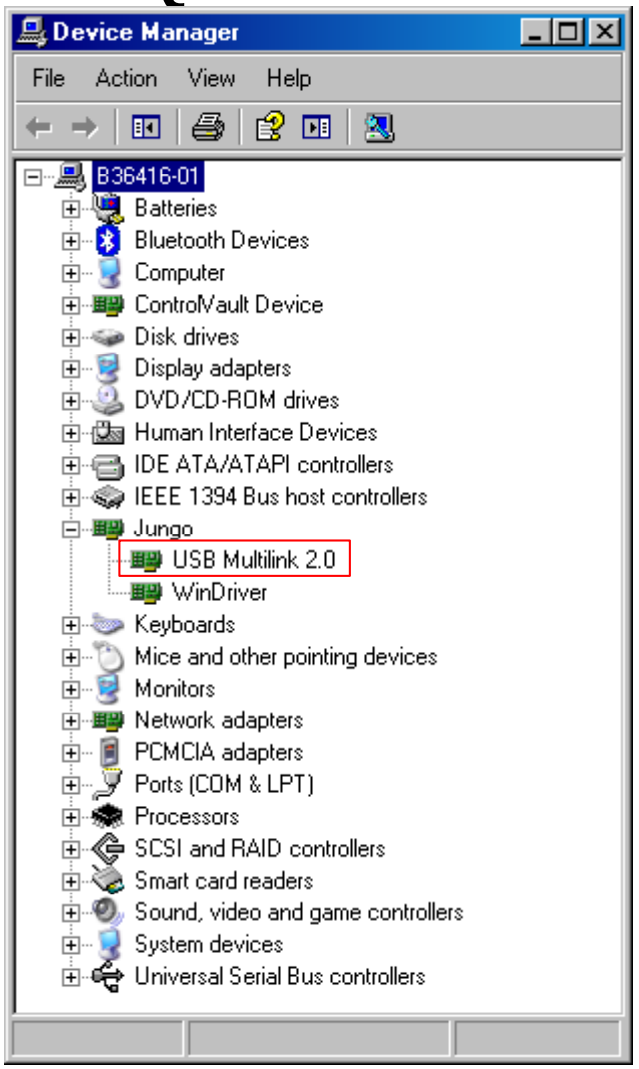
Hardware Setup
USB Qorivva Multilink

- If the USB Qorivva Multilink is used:

The “USB Multilink 2.0” device can be found in your computer device list.



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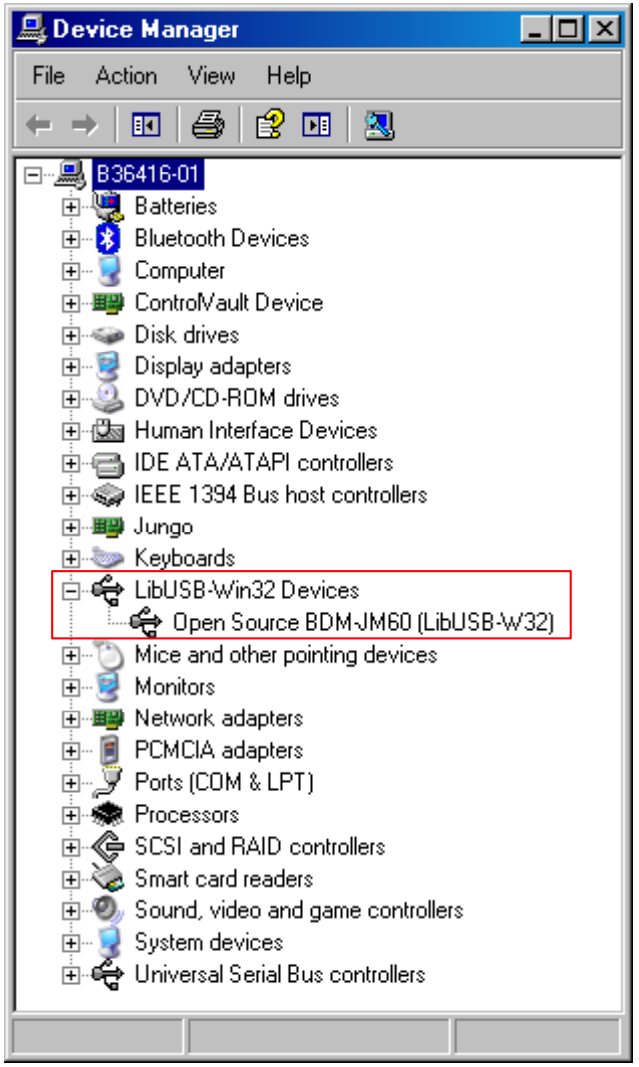
Hardware Setup
TRK-MPC5604B

- If the TRK-MPC5604B board is used:

The "BDM-JM60 (LibUSB-Win32)" device can be found in your computer device list.

- The on-board Embedded OSJTAG is available.



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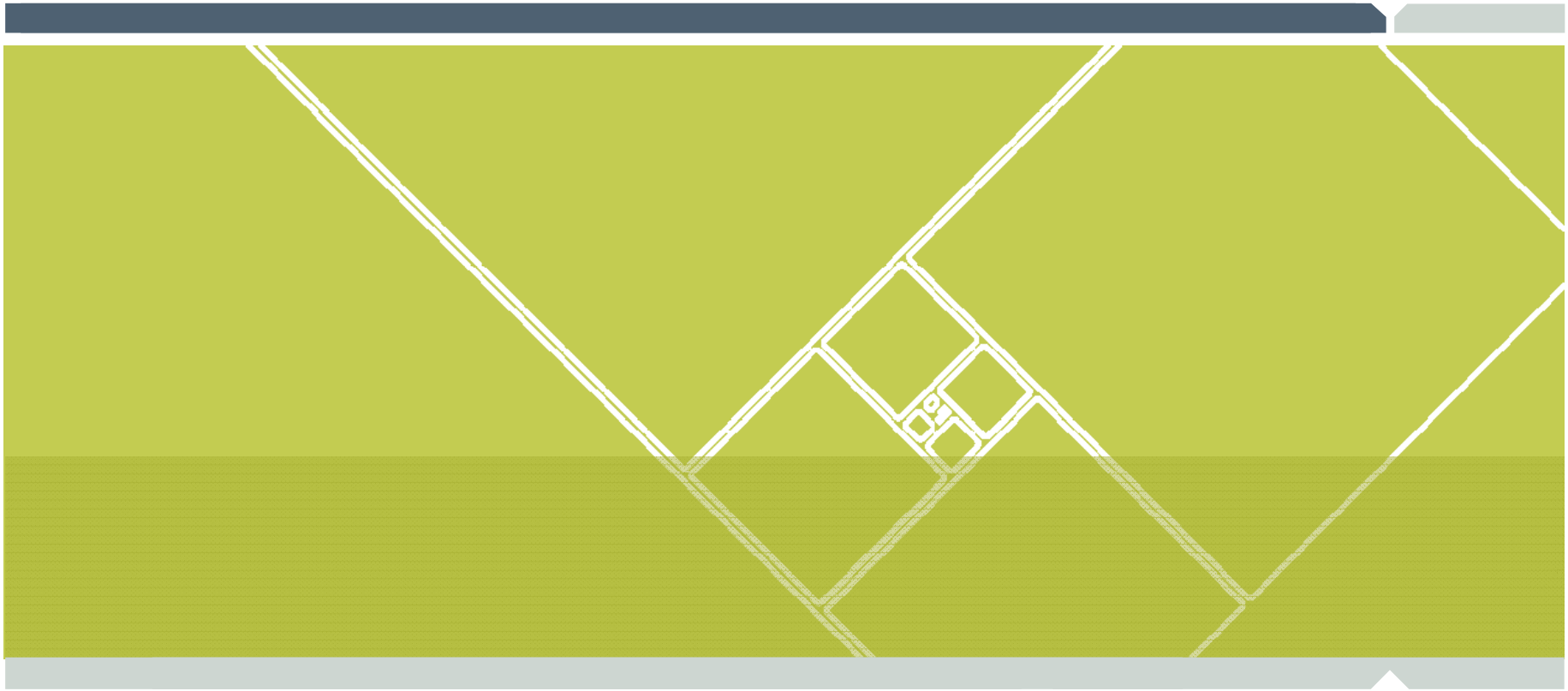
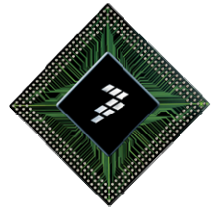


Hands-on Demos



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Hands-on Demos

1. *SIUL GPIO*
2. *System Clock Generation*
3. *Mode Transition Demo*
4. *Low-Power Mode*
5. *Interrupt and PIT*
6. *FlexCAN Lookback(RAppID)*
7. *ADC-EMIOS*

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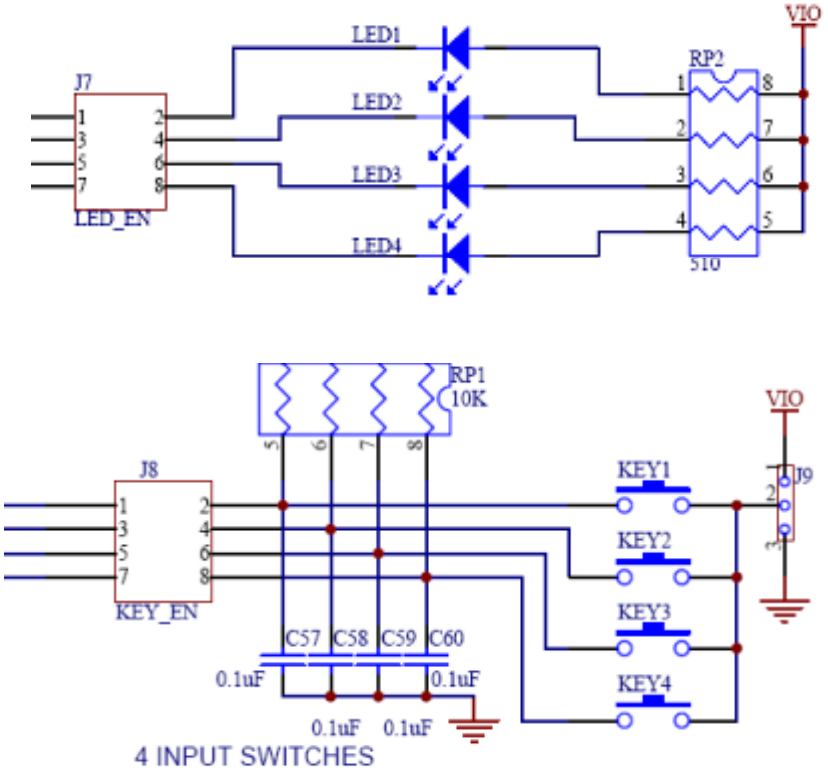
Lab Target:

Through this lab, customer will learn how to configure a PIN to GPIO and to read/write the I/O status. (Base of the rest labs.)



LED	eMIOS_0	MCU Port	SIU_PCR
1	Channel 20	PE4	68
2	Channel 21	PE5	69
3	Channel 22	PE6	70
4	Channel 23	PE7	71

SWITCH	MCU Port	SIU_PCR
KEY 1	PE0	64
KEY 2	PE1	65
KEY 3	PE2	66
KEY 4	PE3	67

Hints:

1. Configure SIU.PCR[n]

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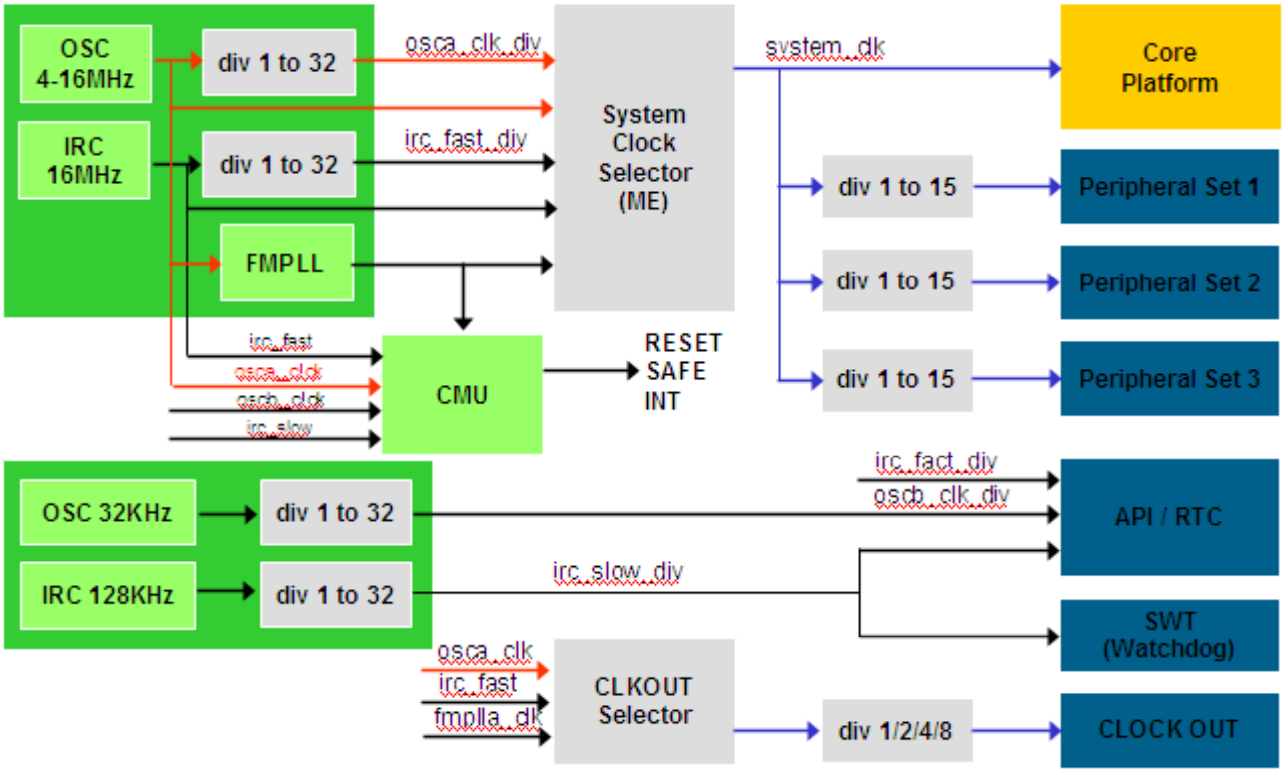
LAB2:System Clock Generation

Lab Target:

Through this lab, customer will learn how to generate the system clock by FMPLL sourcing from external high frequency oscillator.



Hints:

1. Configure the ME.RUN[0]
2. Try these 3 sources
   - IRC (16M)
   - OSC (8M)
   - PLL (64M)
3. Add the LED toggle code to easy check.

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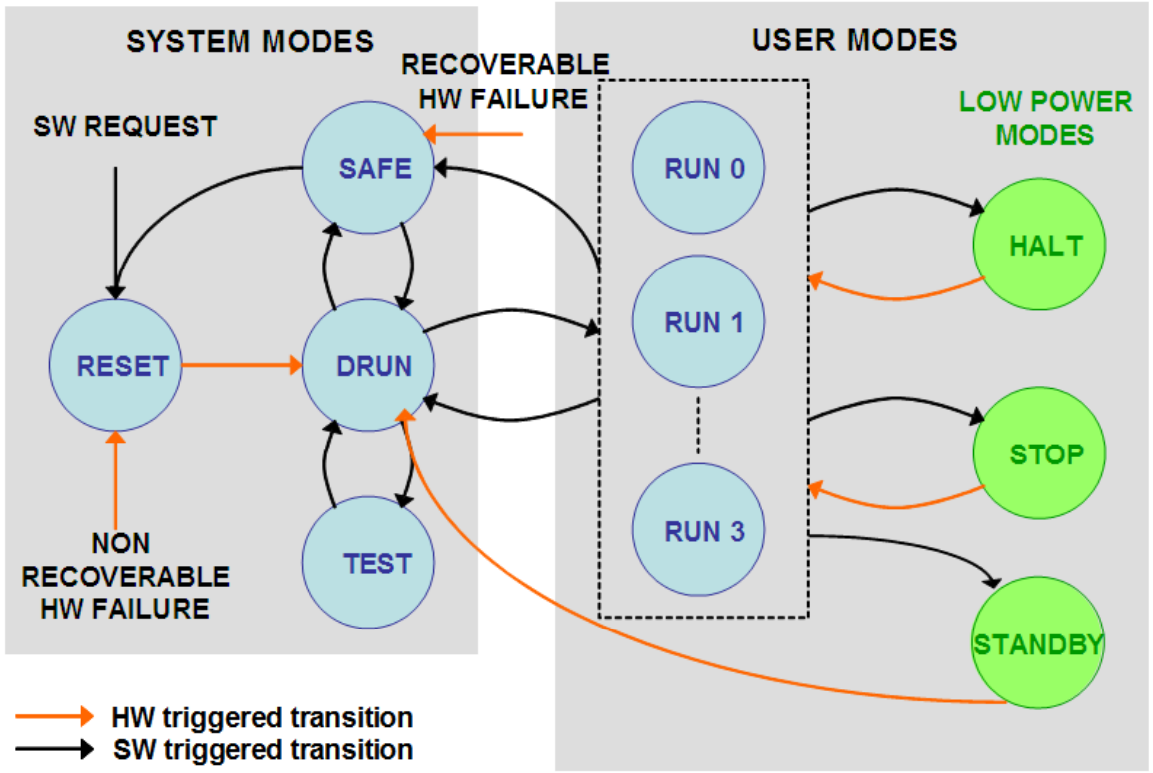
LAB3: Mode Transition Demo

Lab Target:

Through this lab, customer will learn how to put Bolero in a specific mode by either software trigger or hardware trigger.



Hints:

1. DRUN to RUN0, then to switch between RUN0 and RUN3.
2. Configure the registers of
   ME.MER
   ME.RUN[0-3]
   ME.RUNPC[0-7]
   ME.LPPC[0-7]
3. Configure peripheral ME.PCTL[n]
4. Wait for the mode stable before to do the mode transition.

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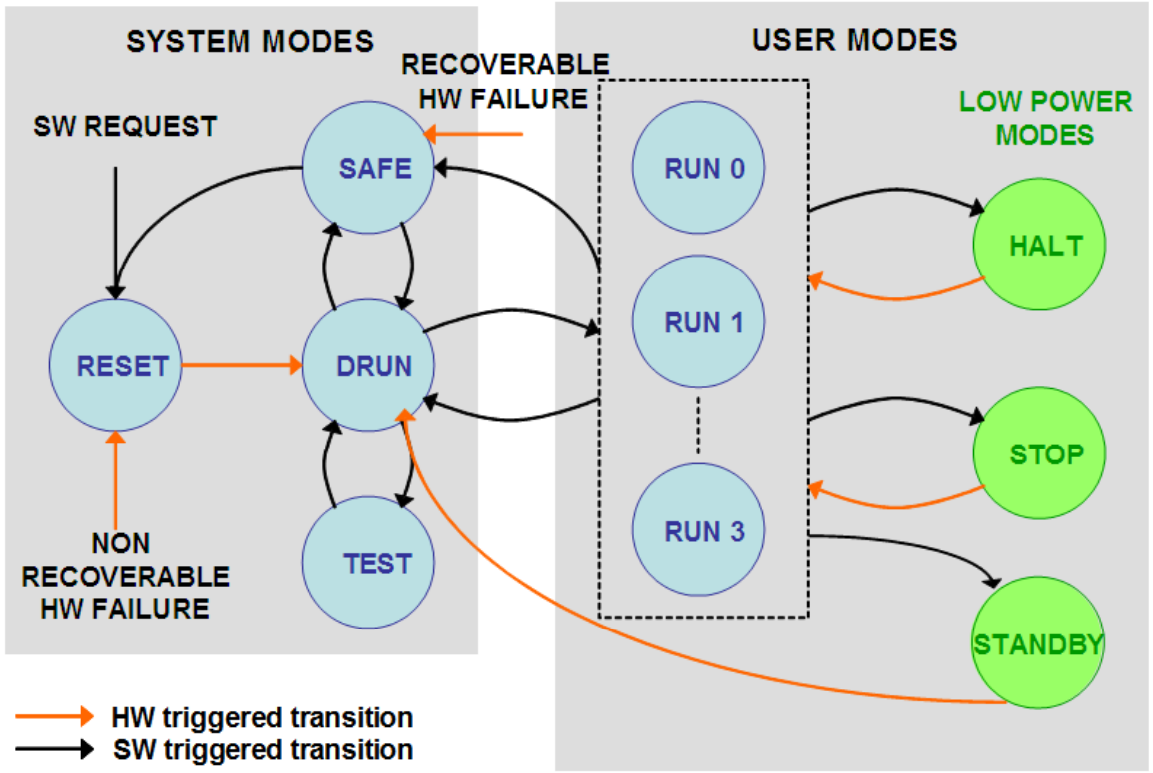
LAB4: Low-Power Mode

Lab Target:

Through this lab, customer will learn how to put Bolero into Standby and then exit the Standby by Wakeup pin or API.



Hints:

1. RUN0 to Standby.
2. Configure Wakeup pin before transfer to standby.
3. Try to use Button4 to enter standby. Wakeup by API.
4. “Modes_LowPower” sample code.

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LAB5: Interrupt and PIT

Lab Target:

Through this lab, customer will learn how to configure a PIT and implement the interrupt service routine.

```
void initINTC(void) {
  INTC.MCR.B.HVEN = 0;          /* Single core: initializ
  INTC.MCR.B.VTES = 0;          /* Single core: Use defau
  INTC.IACKR.R = (uint32_t) &IntcIsrVectorTable[0];
}

void initPIT(void) {
                              /* NOTE:  DIVIDER FROM SYS
  PIT.PITMCR.R = 0x00000001;        /* Enable PIT and c
  PIT.CH[1].LDVAL.R = 64000;        /* PIT1 timeout = 6
  PIT.CH[1].TCTRL.R = 0x000000003; /* Enable PIT1 inte
  INTC.PSR[60].R = 0x01;            /* PIT 1 interrupt
}

void initSwIrq4(void) {
  INTC.PSR[4].R = 2;           /* Software interrupt 4 IR
}

void enableIrq(void) {
  INTC.CPR.B.PRI = 0;             /* Single Core: Lower I
  asm(" wrteei 1");               /* Enable external inte
}
```

Hints:

1. Reuse the sample code of CW. “INTC-SWvector-VLE”.
2. Integrate the LED toggle code from LAB1 into the ISR.
3. Modify PIT period to check the result on board.

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Lab 6 FlexCAN Lookback(RAppID)

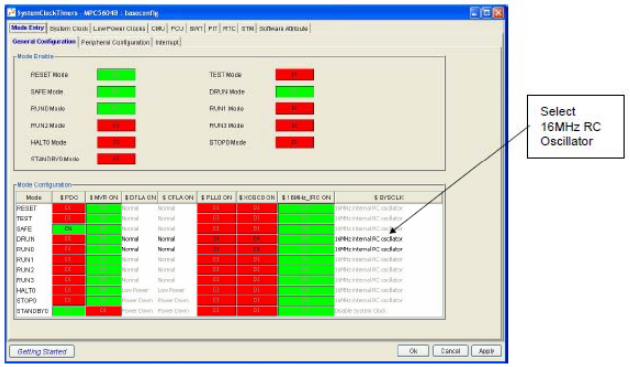
Lab Target:

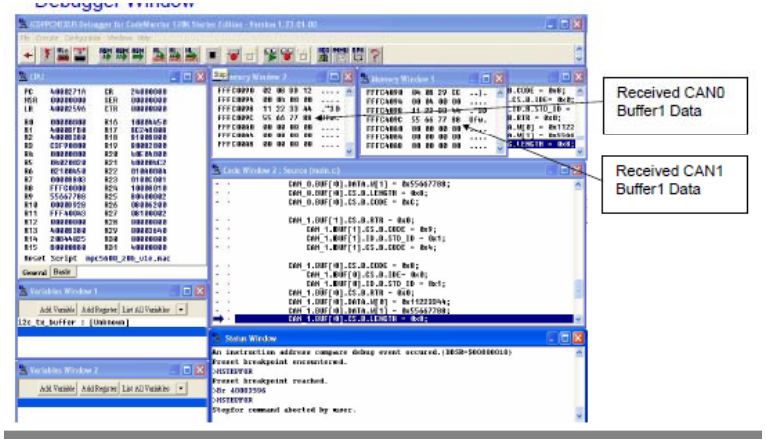
Through this lab, customer will learn how to use RAppID to generate FlexCAN loopback code, compile with Codewarrior and debug on EVB.

Section:

- Getting Started with FlexCAN
- Overview of the steps
- RAppIDJDP GUI Setup
- Code
- Application Execution
- Debugger Window

Detail steps please refer to: RAppID MPC5604B FlexCAN Tutorial located under RAppID install folder: “xxx\560xB\Help\Tutorials\FlexCANTutorial.pdf"





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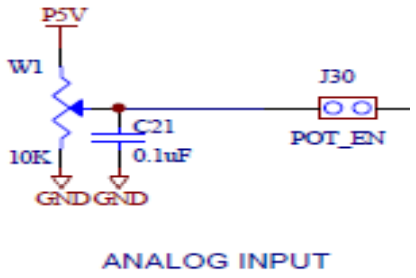
LAB7: ADC-EMIOS

Lab Target:

Through this lab, customer will learn how to capture ADC input and generate PWM signal with EMIOS.

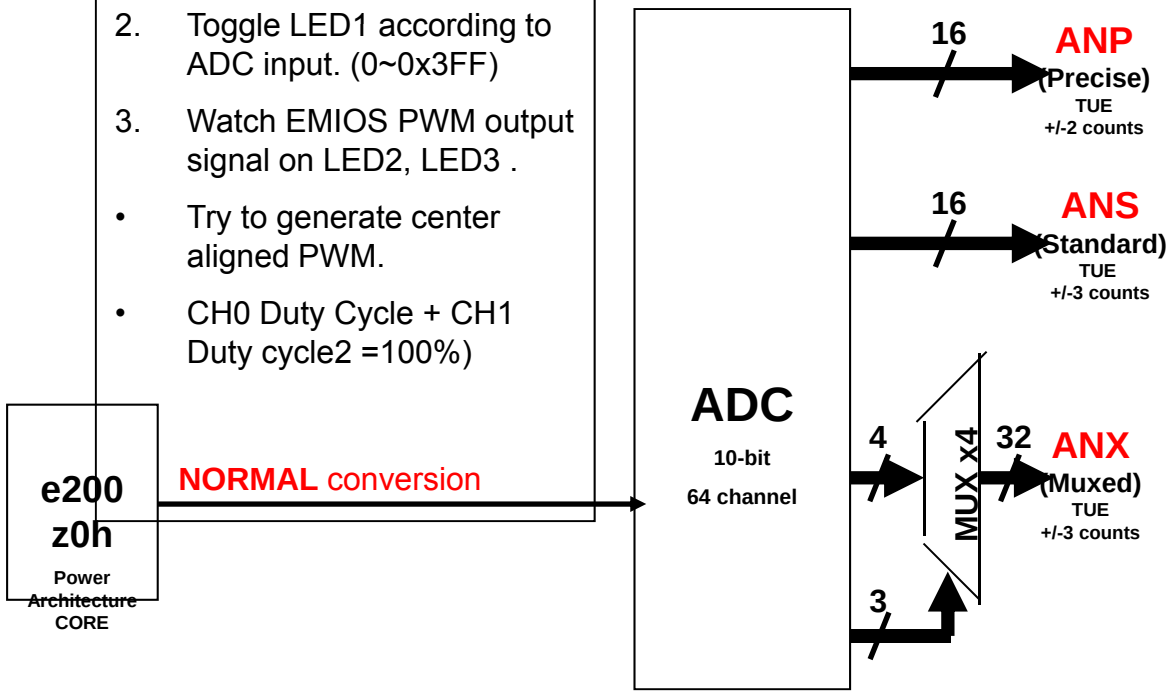


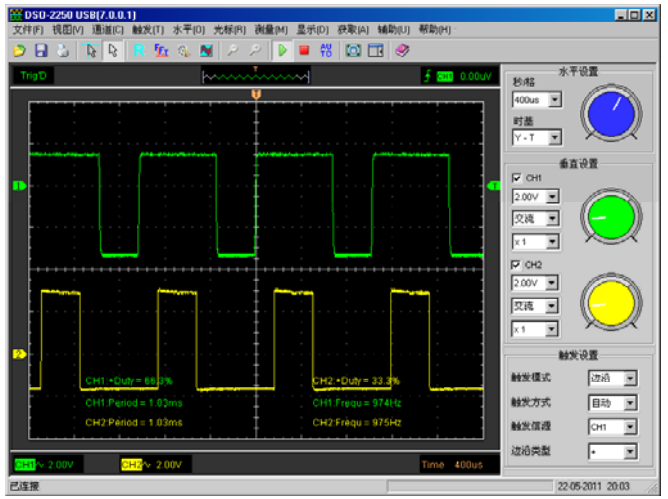
Hints:

1. Configure ADC for software scan mode.
2. Toggle LED1 according to ADC input. (0~0x3FF)
3. Watch EMIOS PWM output signal on LED2, LED3 .

- Try to generate center aligned PWM.
- CH0 Duty Cycle + CH1 Duty cycle2 =100%)

•Connect **J30.2** ADC channel to **P2.5** for variable voltage
(J30.2 is pin nearest W1)





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